
SERMA GROUP
SECURE YOUR FUTURE

SERMA GROUP

STRATEGIC FIELDS OF BUSINESS

SAFETY AND CYBERSECURITY OF SYSTEMS

ELECTRONICS AND MATERIALS TECHNOLOGIES

EMBEDDED SYSTEMS ENGINEERING

ENERGY

MICROELECTRONICS

- Expertise
- Consulting & Auditing
- Design
- Assembly
- Production
- Testing and Qualification
- Evaluation
- Build-to-spec/ Build-to-print
- Through-life maintenance
- Maintaining security conditions
- R&D
- Training

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SERMA GROUP
SUBSIDIARIES AND LOCATIONS

- SERMA Technologies
- SERMA Safety & Security
- SITREND
- SERMA Ingénierie
- AW2S
- KN Systèmes
- SERMA Energy
- SERMA Energy Iberica
- SERMA Microelectronics
- Thin Film Products
- ID MOS
- SERMA Productivity Engineering
- SERMA International

SERMA
PRODUCTIVITY ENGINEERING

ASIC Design & Production

PE
AT A GLANCE

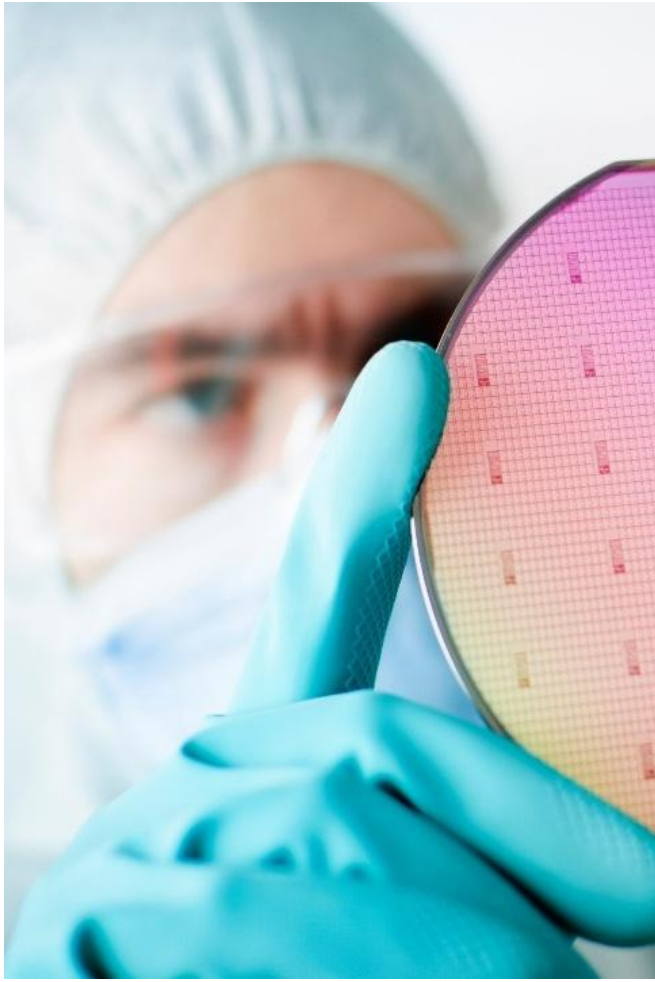
1997
Company establishment

20
Employees Germany (P.E)

>130
ASIC designs

10
new ASIC designs per year

6.2M
units delivered in 2025
(40 customers)



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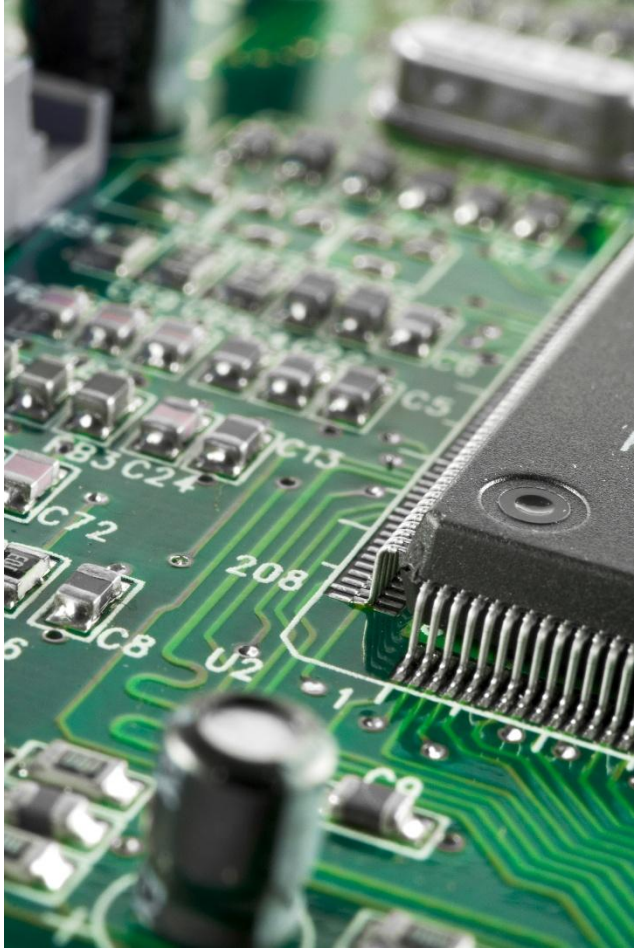
PE
AT A GLANCE

Milestones:

- 1997: foundation of Productivity Engineering GmbH
- 2003: certification according to ISO 9001 & ISO 14001
- 2005: establishment of the IC Design Center Dresden
- 2013: acquisition of PE by „Group Serma“ (>1500 employees)
- 2026: > 130 ASIC-Designs realized



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SERMA PRODUCTIVITY ENGINEERING

PE
AT A GLANCE

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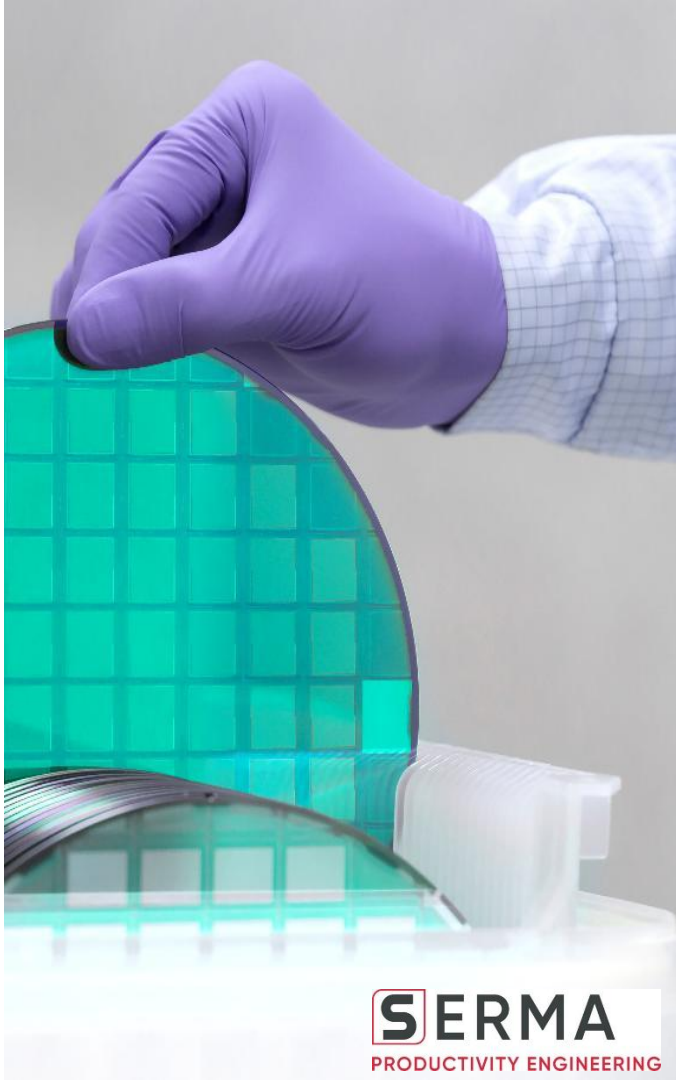
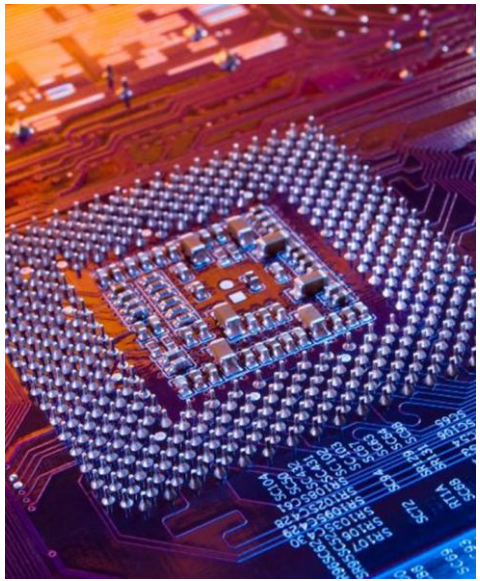
Fabless semiconductor expertise – from design to production

- Strong expertise in mixed-signal ASIC development
- Obsolete circuits migration or redesign
- FPGA migration and conversation into ASICs
- Industrialization and Full long term supply-chain management
- Prototype manufacturing up to scalable series production
- Highly experienced team of engineers located in Dresden
- Privileged access to the SERMA Group's infrastructure



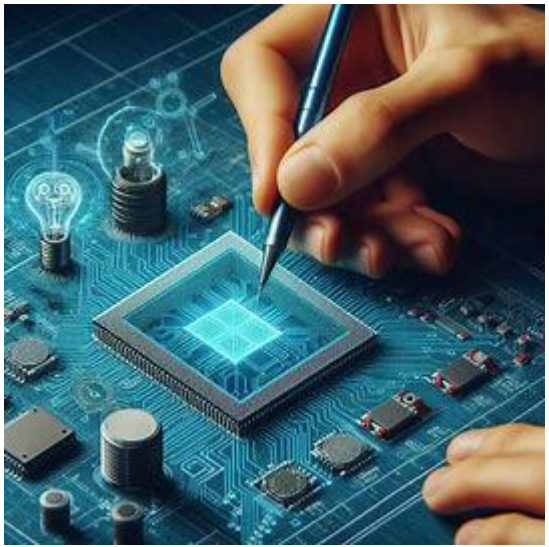
GENERAL EXPERTISE AND CAPABILITIES



- ✓ Sensor signal conditioning
- ✓ Analog IP: LNA, ADC, switched capacitance filters, clock & power management…
- ✓ Ultra-low power design implementations: tracking the nA!
- ✓ High voltage using BCD technologies including SOI: >200V
- ✓ High Temp (175°C standard, >175°C on demand) & Rad Hard tolerant
- ✓ Embedded HALL & TEMP sensors
- ✓ Digital IP: MCU, memories, interfaces…
- ✓ Dedicated methodologies for specific domains: DO254
- ✓ Supporting advanced packaging solutions: SIP, WLCSP

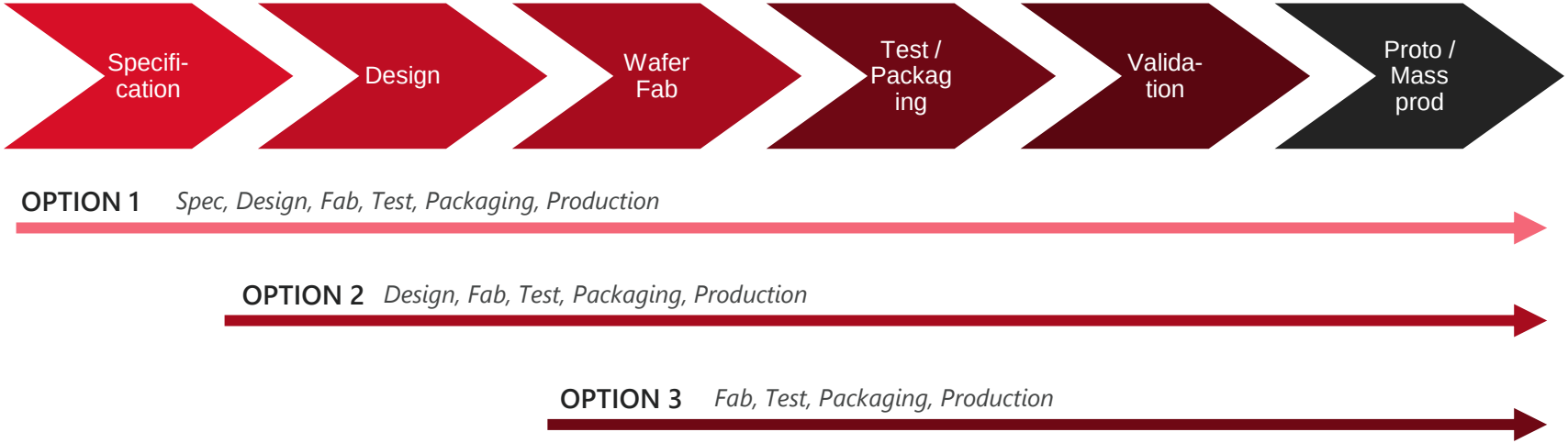
EXPERTISE AND CAPABILITIES
IN SENSORS

- ✓ Interfacing capacitive, piezo resistive, inductive, Hall, temperature
- ✓ Low-noise charge & instrumentation amplifiers
- ✓ ADC solutions optimized for the application up to 22 Bits
- ✓ Analog & digital filtering
- ✓ Sensor data embedded digital processing (custom logic, MCU)
- ✓ Embedded NVM for sensor calibration
- ✓ RISC V architecture and AI implementation for sensor applications



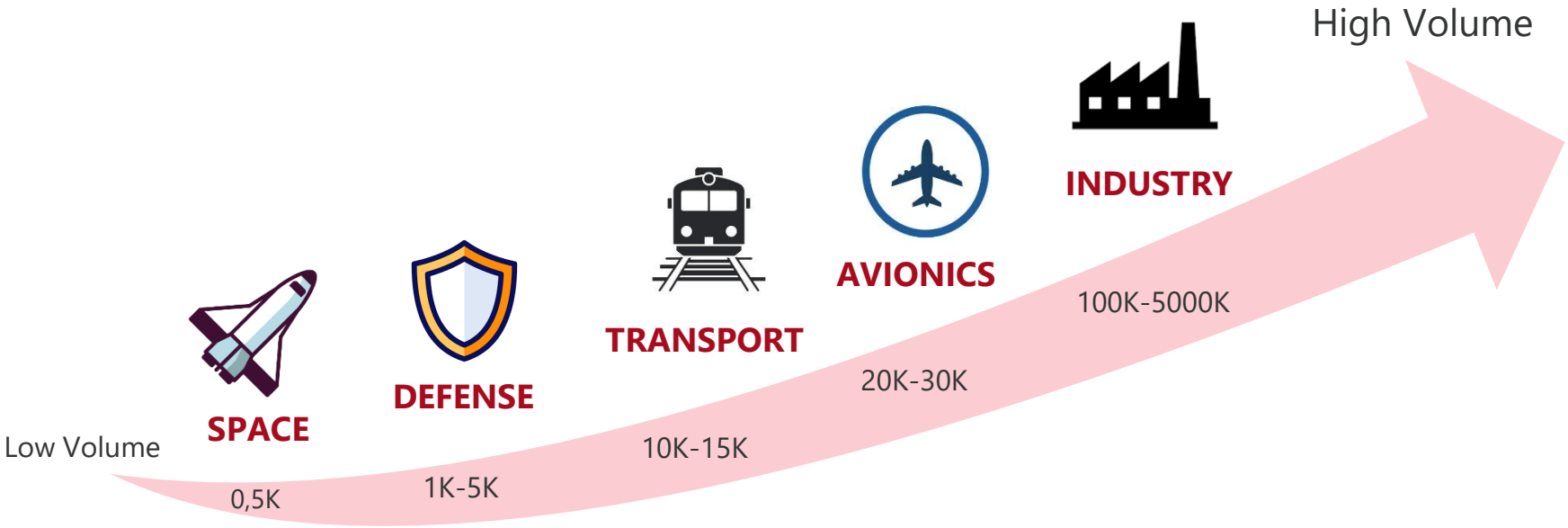
IC/SOC

FLEXIBILITY OF SERVICES



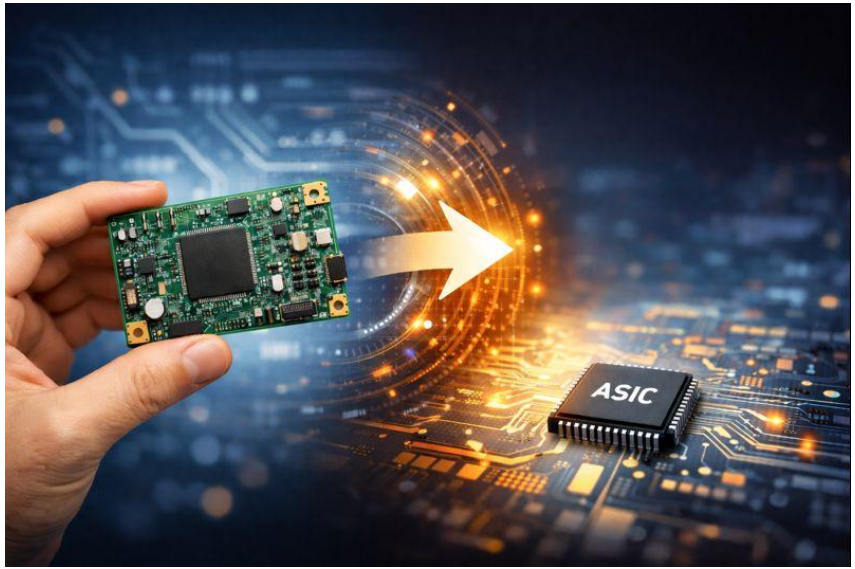
IC/SOC

THE FLEXIBILITY OF PRODUCTION



MOTIVATIONS

TRANSITION TO CUSTOM INTEGRATED CIRCUITS



- IP protection; core function is hard-wired into silicon
- Less dependent on standard component roadmaps and secured supply-chain
- Long term supply assurance (up to 20 years)

- Decreasing power consumption
- Downsize PCB`s and packages
- Minimizing weight
- Capability to work with 5V power supply or even higher

- Reducing BOM and process complexity

- Less material and system consumption

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Cases of FPGA components redesign

OBSOLETE COMPONENTS

PROVEN MIGRATION METHODOLOGY

EVALUATION PHASE

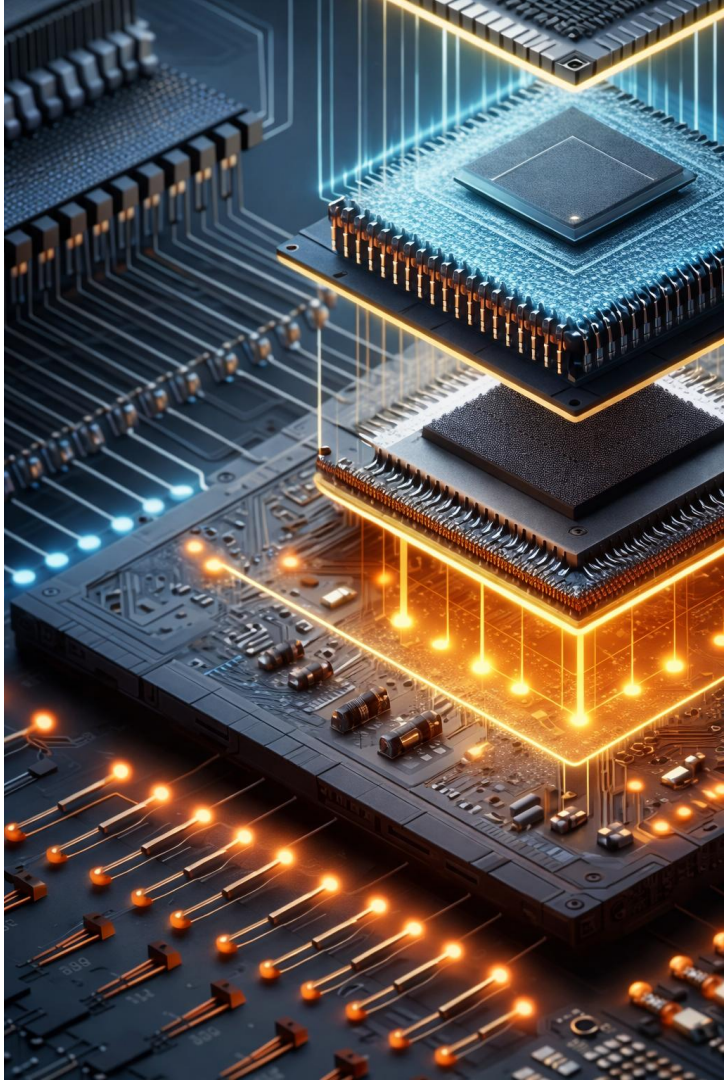
- Electrical and functional characterization of the original circuit
- Analysis of the technological process and packages adapted to design

POSSIBLE INPUT DATA

- Datasheet
- Data base
- Samples

ENVIRONMENT

- Taking into account IC-Board interactions.
- Reproduction of original specification



CASE OF OBSOLETE FPGA COMPONENTS

OBSOLESCENCE MANAGEMENT THROUGH ASIC MIGRATION

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CUSTOMER

Trains

RISKS

Equipment production shutdown in 2 years

THE ISSUE

Critical obsolescence of a FPGA component (XILINX/AMD)

CUSTOMER EXPECTATIONS

- ✅ Offer a long-term solution (minimum 10 years)
- ✅ Fully pin-to-pin compatible
- ✅ Maintain power supply voltage
- ✅ 100% compliant with customer specifications

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CASE OF OBSOLETE FPGA COMPONENTS

SOLUTION DEVELOPMENT FLOW

Input data: Code HDL + Testbenches

Database analysis

Requirements extraction

Technological Process selection (XP018)

Digital Design

Production of prototypes

Testing and characterization

Comparison between original component and ASIC prototype

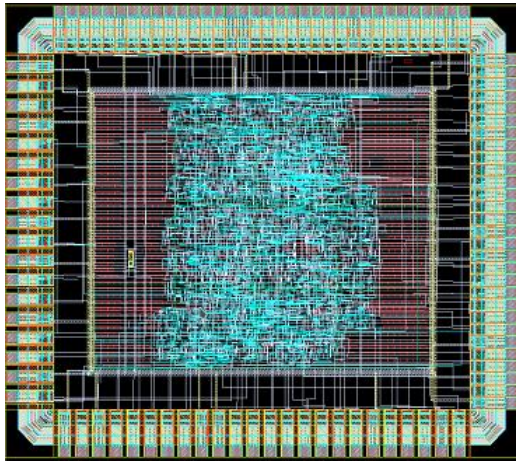
Customer validation

TIMELINE

T 0 + 4 0 w

NRE BUDGET

200-300K€ (simple FPGA)



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CASE OF OBSOLETE FPGA COMPONENTS

FPGA TO ASIC SOLUTION

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Why outsource FPGA migration with PE?

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Extensive experience in FPGA migration

- 25 years of recognized ASIC Expertise (Digital, analog or mixed signal)
- Experienced design team (over 15 years of average experience)
- Over a dozen FPGA migration projects completed
- Privileged access to the SERMA Group's infrastructure
- One-stop supplier from ASIC design to mass production

ASIC solution

- ✓ Immunity against obsolescence
- ✓ Compatibility with the original FPGA
- ✓ Lower consumption
- ✓ Optimization costs
- ✓ IP protection

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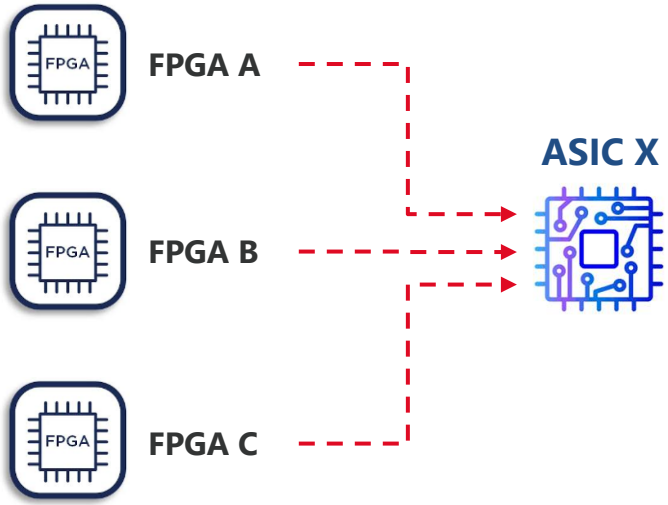
CASE OF REDESIGN FPGA COMPONENTS

MERGE SEVERAL FPGA TO ONE ASIC SOLUTION



- ✅ Reduced unit cost driven by cumulative production volumes
- ✅ Savings in tooling costs
- ✅ Single die supporting multiple package configurations
- ✅ Safety for obsolence

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Example of ASIC Technologies

X-FAB

X-FAB 180NM CMOS TECHNOLOGY PLATFORM AT A GLANCE

	XH018	XP018	XT018 (SOI/DTI)	XS018 (CIS)	XS018 (OPTO)
Core Voltage	3.3V SG 1.8V/3.3V DG 1.8V/3.3V/18V TG	5V SG 1.8V/5V DG	5V SG 1.8V/5V DG	3.3V SG 1.8V/3.3V DG	3.3V SG
High Voltage	10V, 15V 20V, 45V	12V, 15V, 25V, 40V, 60V	10V, 12V, 15V, 20V, 25V, 32V, 40V, 60V, 70V, 85V, 100V, 125V, 100V - 200V, 45V - 375V		
Sensor/ Sensor IF	Photodiode APD/SPAD Low Noise			3T CIS 4T CIS	Photodiode Low Noise
Non Volatile Memory	EasyFuse NVRAM, Flash	EasyFuse, NV Latch, TrimOTP, CEEPROM, EEPROM, Flash	EasyFuse, NV Latch, TrimOTP, CEEPROM, Flash	EasyFuse	EasyFuse
175°C	✓	✓	✓		
AEC-Q100	✓	✓	✓	✓	✓

SG: Single Gate, DG: Dual Gate, TG: Triple Gate

X-FAB

GALVANIC ISOLATOR PROCESS SOLUTION

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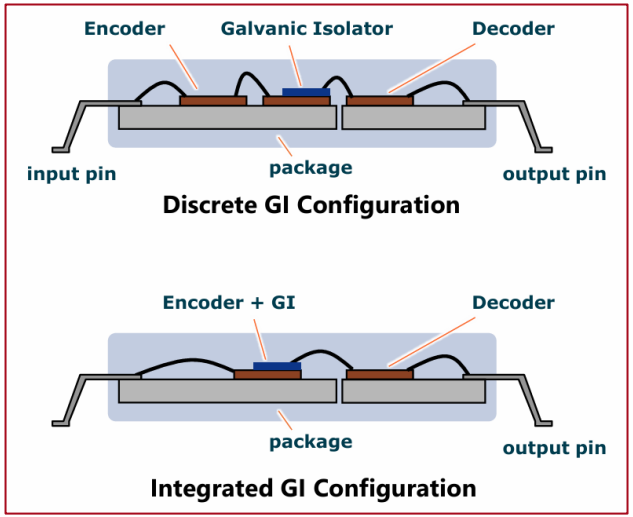
Process for the manufacturing of discrete and integrated coupler devices implemented in 350nm technology XA035

- Different isolation layer thickness options up to 14.3µm
- Isolation strength
  - Suitable for basic and reinforced galvanic isolation
  - Single barrier laid out for V_{IORM} up to 1700 V_{PEAK}
  - Single Barrier laid out for VISO isolation withstand voltages up to 5000 V_{rms} at 50...60 Hz for 1 minute

  Note: Full isolation strength can only be achieved in properly packaged devices
- Process is designed for an operating temperature of up to 175 °C



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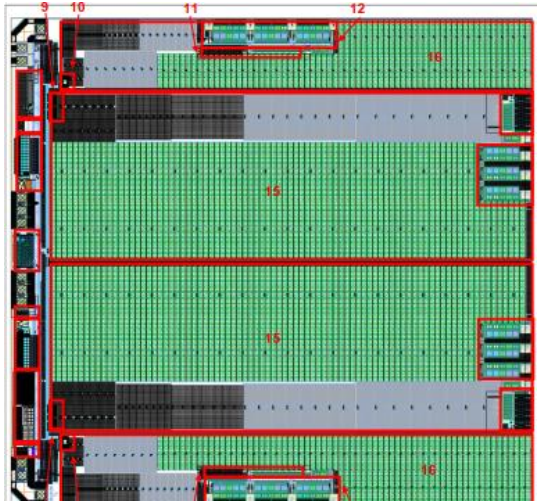
BATTERY POWERED MEMS

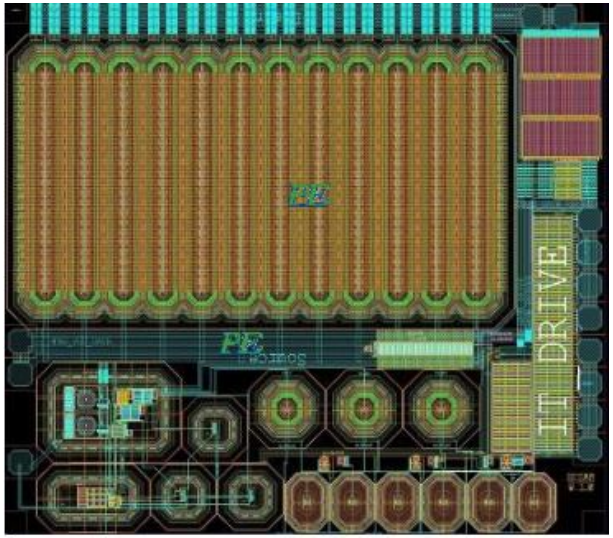
DRIVERS WITH SPI

- The chip is used in a micromechanical application
- The ASIC has to create up to 190V from a battery power supply of 3V
- As battery lifetime is a premium requirement, the chip is optimized for minimum power consumption and efficient output drive rise time
- The design has been performed in 180nm SOI technology
- The device has 12 HV outputs, each of the output must not exceed 2mA
- Chip size is about $2mm^2$



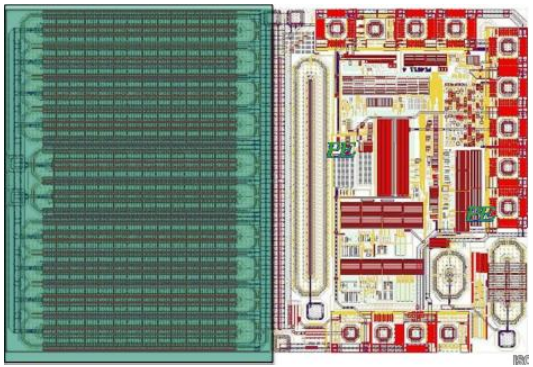
ULTRA HIGH VOLTAGE GATE DRIVER

- The device is used to switch on High Voltage FETs
- Digital interface on board
- Two different output stages were implemented:
- RDS On low side: 20 Ohm
- RDS On High Side: 140 Ohm
- Pmax=500mW
- The design was performed in 700V Ultra High Voltage 350nm technology



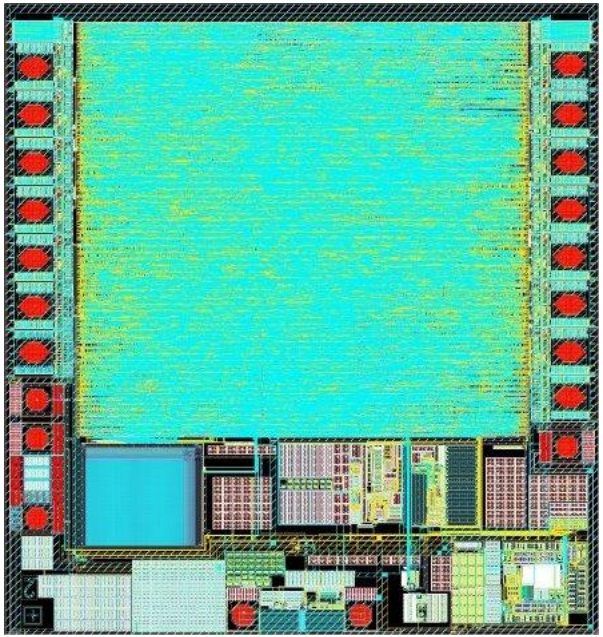
SMART ULTRA HIGH VOLTAGE LED DRIVER

- The devices are used in smart LED-Lighting applications and can be digitally controlled through an SPI
- The device operates on the 110V/220V mains voltage
- The LED output driver transistor is integrated on the chip and can deliver a maximum of 300mA with an RDS On of 13 Ohms
- The design has been performed in 700V Ultra High Voltage 350nm technology
- Chip size is 4,8mm^2



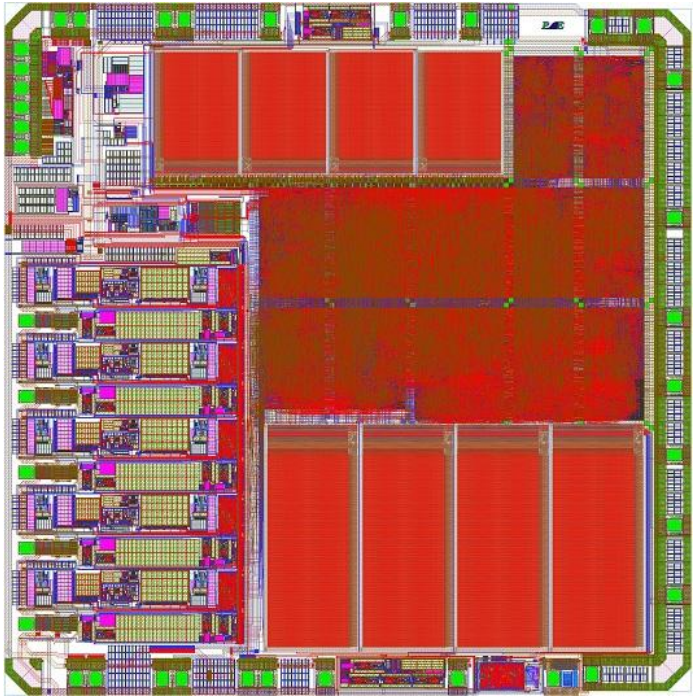
SMART RFID TRANSPONDER

- ISO15693 High Speed protocol
- Customized command structure
- 0,35um CMOS
- 13,56MHz RFID front end
- EEPROM+charge pump
- Operates at 1.1 Volt supply
- Memory Interface
- Microcontroller interface
- Ultra low power design



CAPACITIVE NEAR FIELD SENSORCHIP

- 180nm mixed signal design
- 2 Mio devices
- 32kB embedded Flash
- 12kB embedded RAM
- 32 bit RISC CPU (ARC)
- 5x12 bit ADCs
- Voltage regulators
- RC Oscillators
- AGC Amps
- DC/DC converter
- Universal SPI/I^2C/PS2
- Master/Slave interfaces

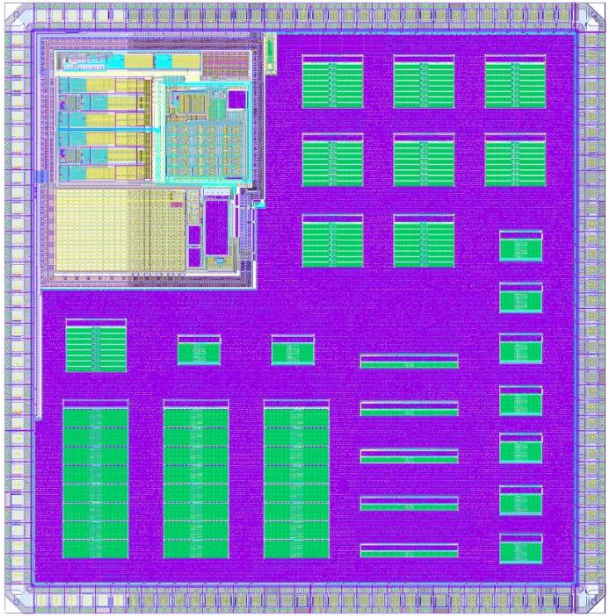


AI TESTCHIP

FEATURES

- 32 Bit RISC-V CPU
- AI Accelerator
- Ethernet MAC
- GPIO's
- UART
- SPI
- ADC & PLL Control
- DDR Controller
- Multiple SRAM's AI Testchip Features

- Analog to Digital Converter
- 2 Instrumentation Amplifier
- Analog Multiplexer
- 400-800 MHz PLL
- 16 Bit PWM @200MHz , 6 channels
- Reference Oscillator
- Real-Time Clock Oscillator
- BandGapReference
- Power-On-Reset
- LDOs
- 142 PADs
- 11mm^2
- 180nm Bulk CMOS



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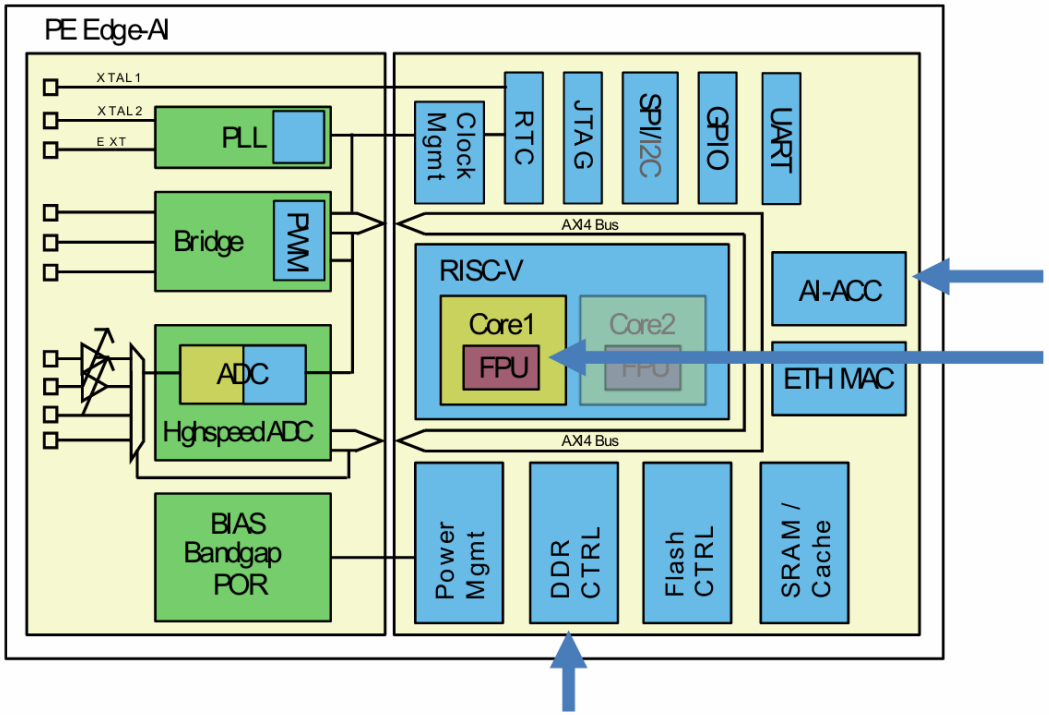
AI TESTCHIP

BLOCK DIAGRAM



CREA PROJECT

THE RISE OF CUSTOM ASIC IN THE ERA OF ARTIFICIAL INTELLIGENCE (AI)

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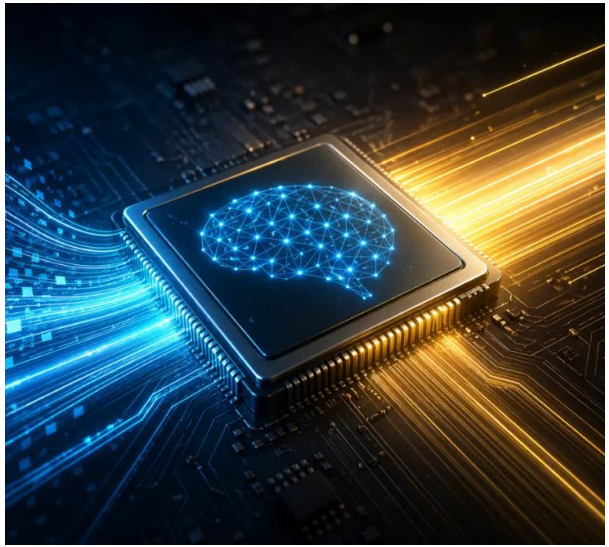
A new generation of smart sensors thanks to Edge AI

One of the major advancements in this transformation is the integration of artificial intelligence directly into devices, close to the data source, without relying on the cloud: this is the principle of **Edge AI**.

Combined with the open RISC-V architecture and specialized hardware accelerators for AI, this approach enables the design of smart sensors that deliver:

- Reduced latency: Real-time processing
- Lower energy consumption: Fewer data transfers
- Enhanced security: Sensitive data kept locally
- Simplified systems: Reduced cloud dependency
- All while cutting costs and system complexity

This evolution shifts sensors from passive to intelligent, enabling them to understand their environment and adapt over time.



For more information visit:

[The rise of custom ASIC in the era of Artificial Intelligence (AI)]

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