
SERMA GROUP
SECURE YOUR FUTURE

OUR MISSION

SECURITY AND RELIABILITY
OF ELECTRONIC, INFORMATION, POWER AND TELECOM SYSTEMS

As an independent and multi-sector global player,
we can support you throughout the life cycle of your products and services

SECURE YOUR FUTURE

INDEPENDENT AND FAST-GROWING PLAYER TO SERVE ALL INDUSTRIES

+30
years of experience

1400
engineers and technicians

30
sites in Europe, Tunisia and USA

70M€
of industrial facilities
Investment > €4M/year

25 000 m²
of industrial facilities: laboratories, production zones, cleanrooms, test platforms

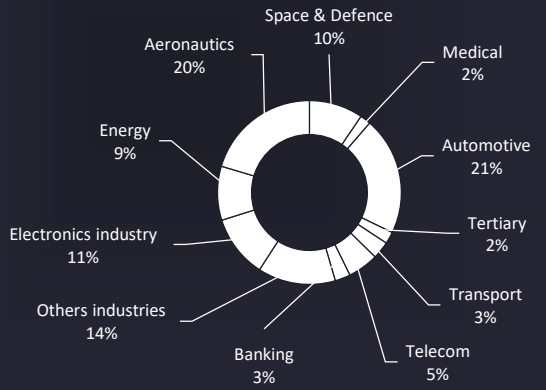
60%
of capital held by managers and employees

R&D
20 projects per year

Certifications
quality, safety and environmental qualification and approvals

A continuous growth (M€)

A multi-sector positioning (% turnover)

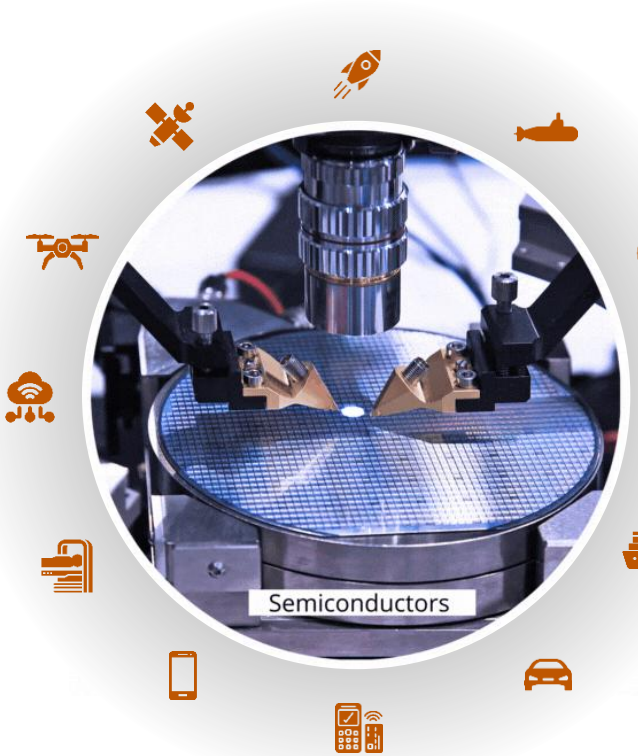


OUR LOCATIONS

SECURE YOUR FUTURE

100% SERVICE

- ELECTRONICS AND MATERIALS TECHNOLOGIES
- SAFETY AND CYBERSECURITY
- EMBEDDED SYSTEMS
- MICRO-ELECTRONICS
- ENERGY



- Expertise
- Consulting & Audit
- Design
- Microelectronics assembly
- Production
- Testing and qualification
- Evaluation
- Build-to-spec/ Build-to-print
- Through-life maintenance
- Maintaining security conditions
- R&D
- Training

TRANSPORT AERONAUTICS SPACE AUTOMOTIVE ENERGY TELECOM & CONNECTIVITY MEDICAL DEFENCE BANKING

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ELECTRONICS AND MATERIALS

TECHNOLOGIES

Expertise in electronics technologies, manufacturing processes, and materials characterization laboratory

Die
Components
Boards & PCB
Materials
Power module
RF

225 employees (Dr, Ing, Tech)
7 000m² of laboratories on 8 sites
2,3M€ of annual investment
10 000 analyses per year
800 customers
R&D and collaborative projects

Electrical & environmental testing

- Electrical testing (analogue, digital, mixed-signal, power, RF) of components, boards, systems
- Qualification tests, reliability, endurance, robustness, etc.
- Electrical modelling
- T&H climatic chambers, HAST,
- Thermal shock, temperature cycle testing, power cycling, HALT, vibration shakers, etc.
- Radiation tests TID, SEU

Physical analysis

- Expertise
- Batch inspection and counterfeit detection
- Failure analysis
- Construction analysis
- Die analyses: Si, SiC, GaN, GaAs, etc. with SEM, FIB, TEM...
- GaN, circuit edit for ASIC

Surface analysis

- All materials
- Surface characterisation
- Physical-chemical analyses
- XPS, SSIMS, DSIMS, GD-OES, SEM-FEG, FTIR Microscopy, etc.

Accreditation n°1-7192
Scope available on www.cofrac.fr

Reverse engineering and semiconductor expertise (US)

- Failure analysis and Construction analysis of IC and PCB
- Services work such as Decapsulation, Cross-section, etc...
- Qualification and DPA work
- Reverse Engineering and Circuit Extraction

Consulting and Training

- Auditing of assembly processes
- Industrialisation
- Obsolescence management
- Systems reliability, HM/PHM, associated models (with AI)
- Root cause analysis and problem-solving support
- Training (Qualiopi)

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ENERGY

Test, validation, reliability and qualification engineering for energy systems and subsystems

Batteries
E-Motor
Hydrogen
Systems (solar panels)
Power electronics
Power components

20 000m² of tests platform

+500 electrical channels

2MW maximum production

Physical and chemical analysis Laboratories

Testing: performance, reliability and qualification

- Electrical functional, validation, qualification and endurance testing
- Abuse tests* (ECE R100, UL1642, UN 38.3…)
- Environmental testing
- Mechanical testing

SERMA Technologies
Accreditation n°1-7191
Scope available on www.cofrac.fr

Analysis, Consulting and Expertise

- Support for product design and industrialization
- Audit of assembly processes
- Qualification, reliability, HM/PH and models
- Technological and failure expertise and analysis
- Technological choices and benchmarking
- Full construction analysis and material electrochemical characterization
- Failure analysis and problem-solving
- Physical-chemical, gas, post-mortem analyses etc.
- Multiphysics simulation

Engineering

- Definition, installation and commissioning of test engineering centres
- Definition and design of turnkey test benches
- Implementation of BMS algorithms and validation

*In partnership with CEA

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EMBEDDED SYSTEMS
ENGINEERING

Consulting engineering, design office and production of electronic equipment and embedded software

Sensors
Boards
Power
Opto-photonics
Embedded systems
Embedded software
RF Telecom

3000m² of design office, production facilities and workshop

8 sites

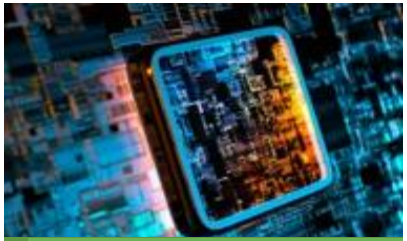
Certifications
ISO 9001 / EN 9100 / ISO 14001

Consulting

- Provision of in/ex-situ advice and expertise
- System, software and electronics hardware engineering
- All activities over the product or project life cycle

Design office

- Board and equipment (build-to -spec)
- Models and prototypes
- Critical systems up to DAL A/SIL 4
- Expertise :
  - Digital/analogue
  - RF, Signal processing
  - FPGA
  - Embedded software



Production

- Embedded equipment according to customer specifications (build-to-print)
- Supply chain management
- Integration/final testing
- Small and medium production runs
- PART 21G

Through-life maintenance

- Repair Centre
- Obsolescence management
- Retrofit management: logistics engineering and technical production
- PART145, FAR145, CCAR145, CAR573

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CYBERSECURITY & SAFETY OF SYSTEMS

Consulting and expertise across the entire systems value chain (products, infrastructures, applications and websites)

Information systems

Industrial systems

IoT systems

Embedded systems

Cybersecurity

audit (qualified PASSI - RGS/LPM), GRC, SOC, and integration of solutions

Security laboratory

accredited ITSEF, FIPS, PCI, SESIP, private schemes, and formal methods

Safety

system, hardware, software, and formal verification of properties

Governance, consulting and compliance

- Governance: inventory of fixtures, BCP, PSSI, PAQS, drafting of the documentary base, etc.
- Consulting: Secure by design, implementation of ISMS, operational safety analysis, etc.
- Compliance: assessment and diagnosis of security levels and compliance with existing security standards (ISO 2700X, ISO 21434, ISO 26262, IEC 62443, etc.)

Offensive security

- Security evaluation laboratory (Common Criteria, FIPS, SESIP, EMVCo, etc.)
  - Public and private schemes
  - Translation: Software, Hardware, and Cryptography security consulting
- Technical audit: intrusion testing, PASSI, PASSI LPM, code review, vulnerability assessment, reverse engineering, configuration review, architecture review

Defensive security

- SOC (24x7) and security incident response
  - EDR, XDR, SOAR
  - Managed cecurity equipment services
- Integration of cybersecurity solutions
  - Audit, research and consulting
  - Technical expertise
  - Support, maintenance and helpdesk services

MICROELECTRONICS

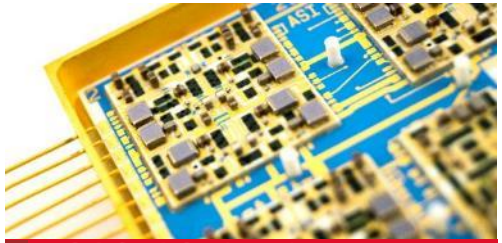
Microelectronics solutions for various customer needs

ASIC
Hybrids
Ceramic substrates
System in package
RF Hyper MMIC
Power module

design office
design and industrialisation

1000m²
of production cleanroom space

Testing laboratory
electrical and environmental

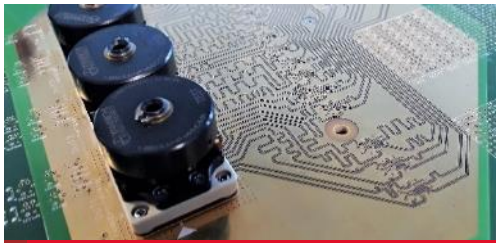


Design

- ASIC, Hybrids
- Mixed-signal integrated circuits, analogue and digital
- Specific applications: high T°, radiation, etc.
- Cloning of obsolete components
- DFM / Process brick development

Production and assembly

- Wafer cutting, chip placement, bonding, etc.
- Hermetic/plastic packaging
- Special processes
- Strategic storage
- Outsourcing or sovereign supply chain
- 20 million parts per year (ASICs)



Testing

- Environmental screening
- Development of electrical tests
- Electrical characterisation and testing in production
- Failure analysis and expertise
- Reliability and Qualification of batches (test design and performance)

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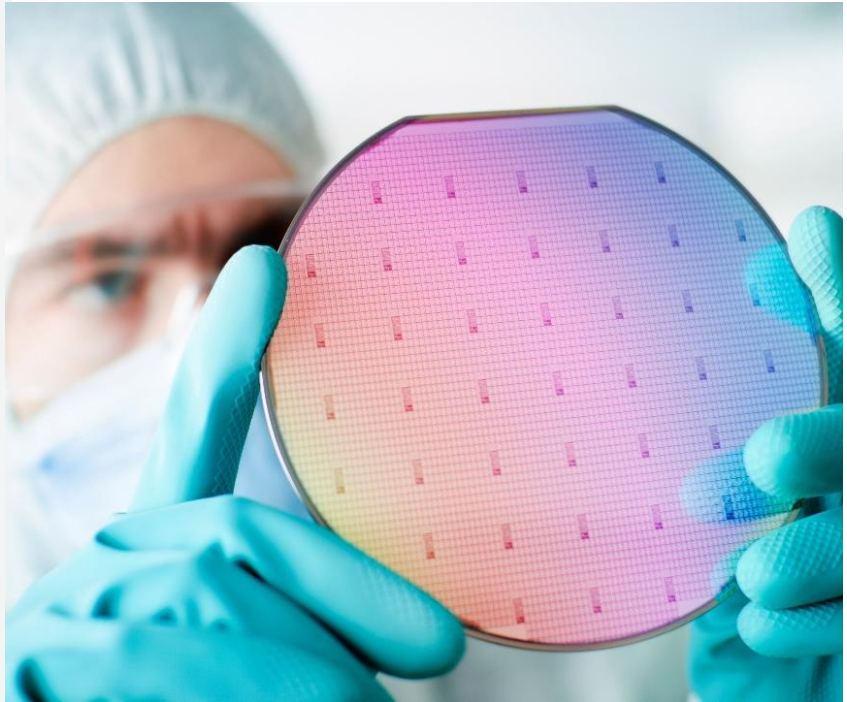
ID MOS & PE GMBH
AT A GLANCE

SECURE YOUR FUTURE

Fabless Semiconductor companies



23M€
Turnover in 2024

40
employees in France (ID MOS) & Germany (P.E)

250
ASIC design history

10
new ASIC designs per year

22M
units delivered in 2024 (80 customers)

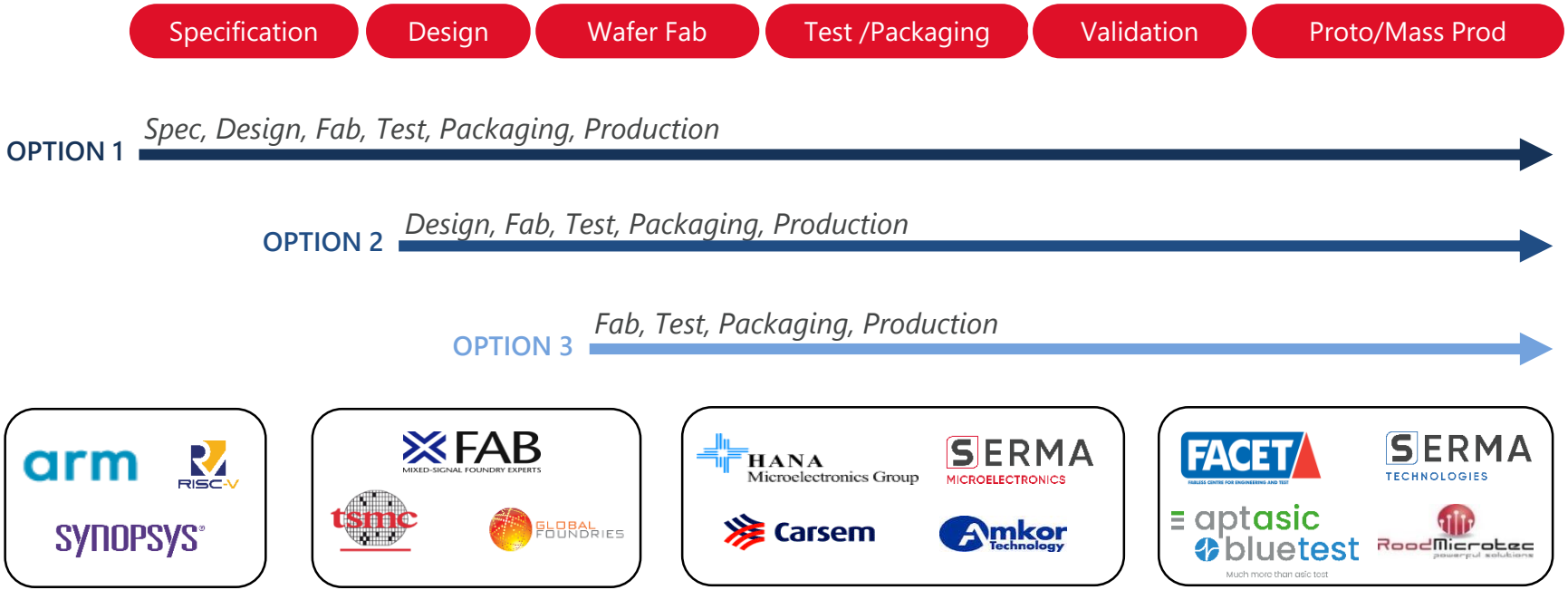
30+
engineers design resources

- Technologies ranging from 1µm down to 55 nm
- Dedicated methodologies for specific domains: DO254, ESCC9000, AEC-Q100...
- Core business:
  - SOC Mixed-signal & Digital microelectronics (ARM Design partner)
  - Technologies for harsh environments (low, high temperature & space)
  - Obsolete circuits redesign (ASIC, FPGA or standard products)
- Full supply-chain management (wafer sourcing, probing, packaging, test & packing)
- Sales offices in France, Germany & Italy
- ISO9001 / ISO14001 certified

arm
APPROVED DESIGN PARTNER

IC/SOC

FLEXIBILITY OF SERVICES



SERMA
MICROELECTRONICS

Microelectronics assembly and production of ceramic substrates

MICROELECTRONICS
ASSEMBLY HOUSE

90
employees

20M€
Turnover
in 2024

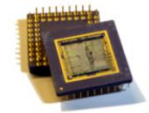
30
years heritages in
back-end services
(wafer treatment,
assembly and test)

Substrates design and production

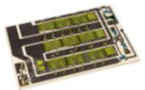
Wirebonding + SMT capabilities

Dice supply and secure storage

We serve customers with constraints:
- **Low Volumes (access constraint)**
- **Environment (reliability needs)**
- **Geopolitical (sovereignty)**
- **lifetime (Perennity)**


Single Chip Modules


MCM / Hybrids


Power modules

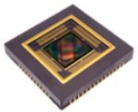
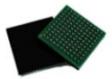


Image detectors


CCGA

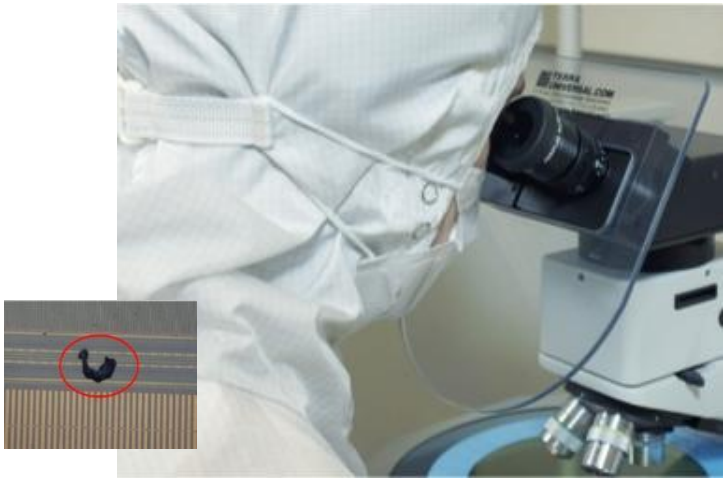

Thick films


Enhanced plastic


Thin film

SECURE YOUR FUTURE

WAFER TREATMENT
DIE MANAGEMENT



DIE VISUAL INSPECTION according to:

- ESCC 20400
- MIL-STD-883
- MIL-STD-750
- Customer specification

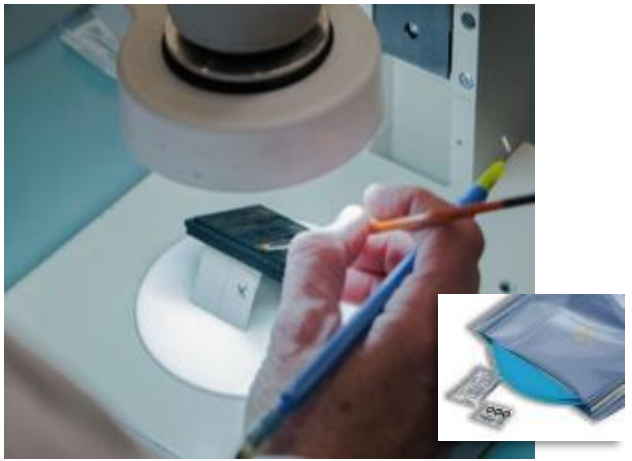
WAFER SAWING

- 8'' DISCO sawing machines
- Wafer mounting on adhesive/UV films on frames
- De-ionized water station/CO2 Bubbler
- Materials: Si, GaAs, Ceramic, Glass, Sapphire, SiC, GaN, etc.
- Loading in waffle packs / gel packs

DICE SUPPLY
& LONG TERM STORAGE

DICE SUPPLY

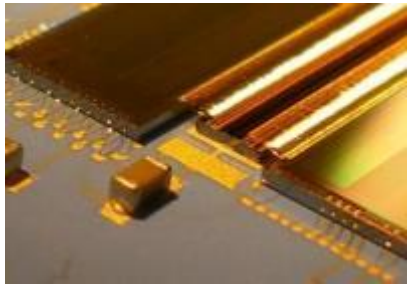
- Supply in wafer form or die form
- Reconditioning / cleansing
- Delivery in waffle packs or gel packs
- Worldwide sourcing network



LONG TERM STORAGE

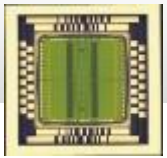
- Dry air / Nitrogen flux
- Temperature / humidity monitoring
- Anti intrusion lock-in system
- Fireproof warehouse

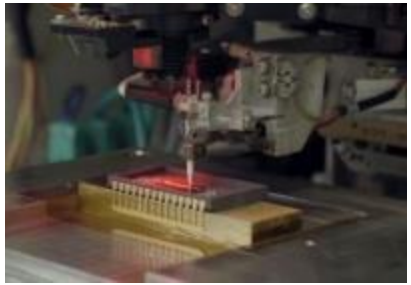
A VARIETY OF ASSEMBLY PROCESSES



DIE ATTACH

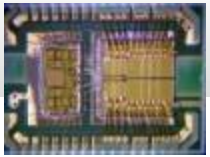
- Adhesive (conductive, insulating)
- Eutectic
- Soft solder
- Silver sintering

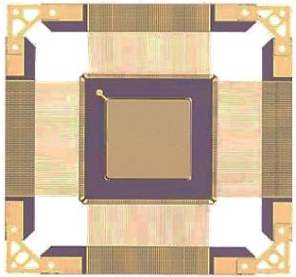




WIREBONDING

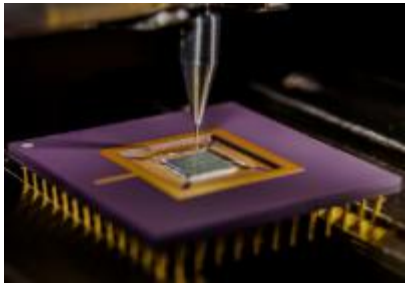
- Wedge bonding (Al/Au 17 to 75 µm)
- Ball bonding (Au 17 to 75µm, Cu 25µm)
- Heavy wire bonding (Al 125 to 500 µm)
- Cu/Pd
- Flip chip





SEALING

- AuSn sealing
- Seam welding
- Epoxy or siliconGlobe top
- Silicon Gel casting
- Adhesive Glass lids



SCREENING

- Bond Pull / Die Shear
- PIND TEST
- X-Rays
- Seal test
- Laser marking
- Environmental tests (HTSB, TC, Const acc..)

HIGH RELIABILITY CIRCUITS
BASED ON CERAMIC SUBSTRATES

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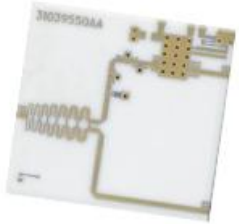
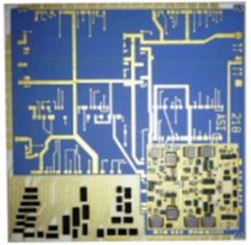
THIN FILM TECHNOLOGY

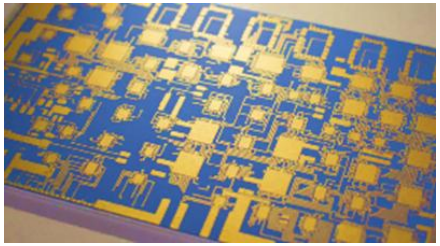
- Mainly used in microwave products
- Based on sputtering and pattern etching processes
- Very good manufacturing accuracy (15µm +/-2µm line width)
- Wide plating possibilities (TiW / Pd / Au / Ni / Cr / Cu / other)
- Resistive layers based on NiCr or Ta2N
- Other substrates : Alumina, Ferrite, Quartz, Rogers



THICK FILM TECHNOLOGY

- For power applications and harsh environment
- Convenient for extreme temperatures
- Based on screen printing process
- Multi layers design possible
- Resistor layers with high accuracy (trimming
- Other substrates : alumina, DBC, LTCC/HTCC





FOCUS on PLASTIC PACKAGES

TYPICAL BGA QUALIFIED FOR AEROSPACE

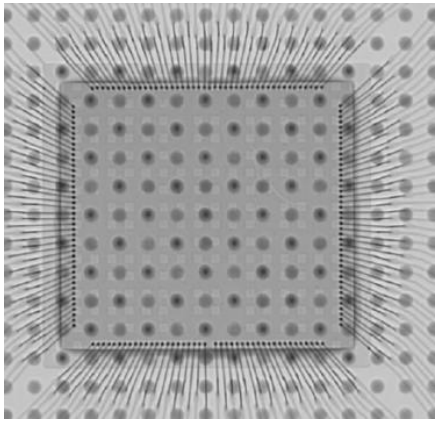
► **Qualification flow based on ESCC9030**

► **:**

- **Pre-Conditionning MSL3**
- **Pressure Cooker Test**
- **uHAST 130°C / 85% / 33PSIA**
- **Thermal Cycling x500 at -65/+150°C**
- **HTS 500h at 150°C**

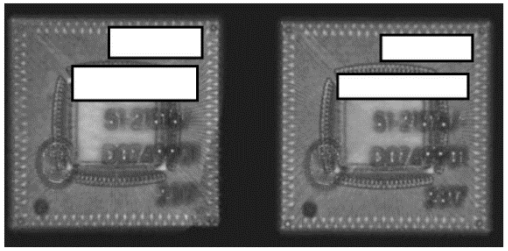
► **100% done by Serma Technologies,**

Including standard construction analysis at the end !

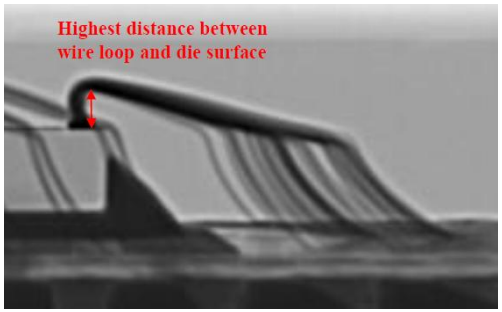


BGA size : 24x24mm
Die Size: 11x11mm

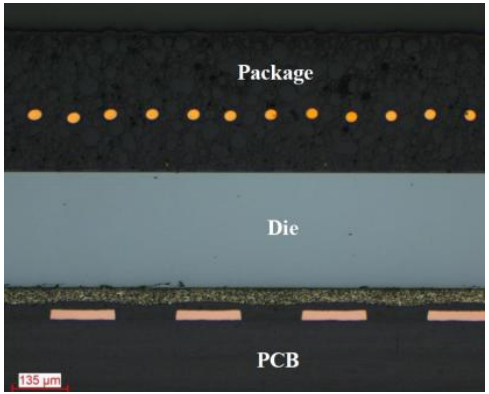
CSAM



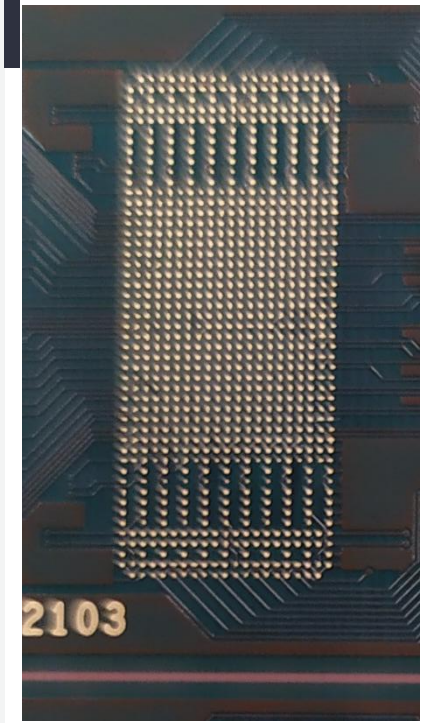
XRAY

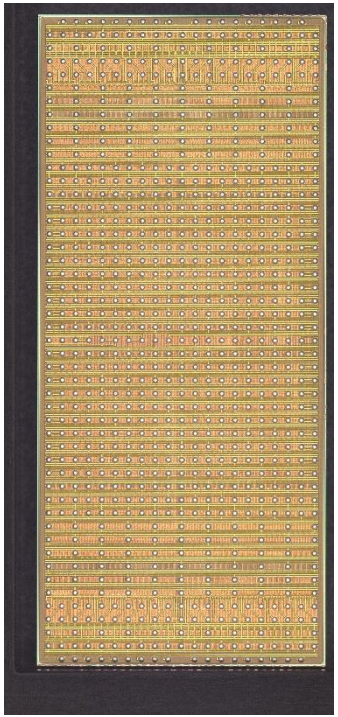


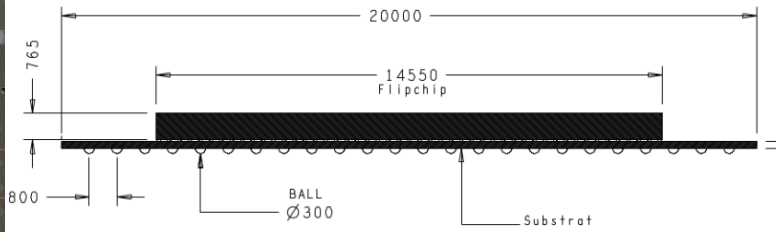
Cross-section



TYPICAL FLIP-CHIP BGA QUALIFIED FOR DEFENSE

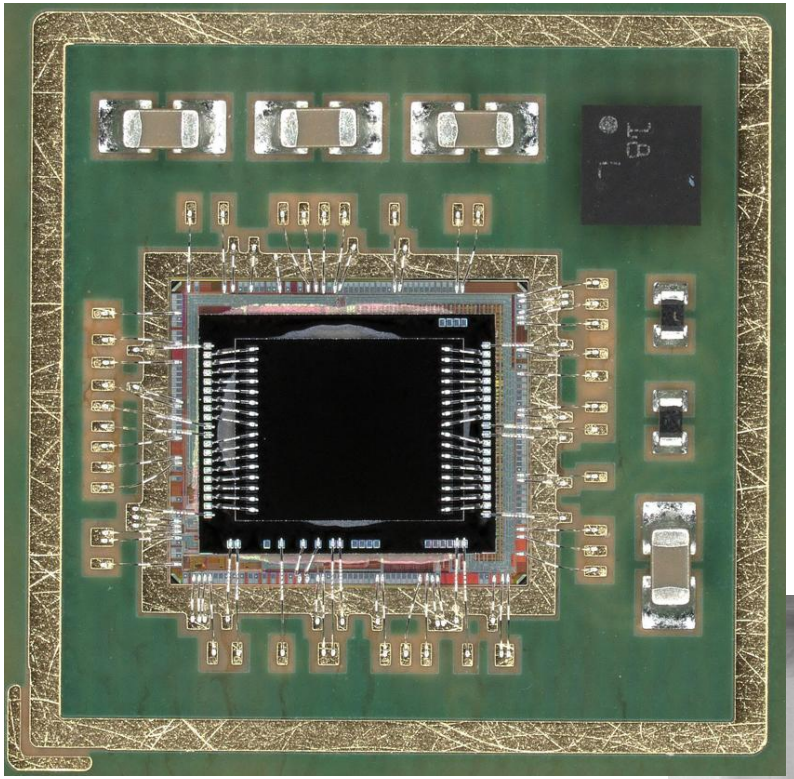


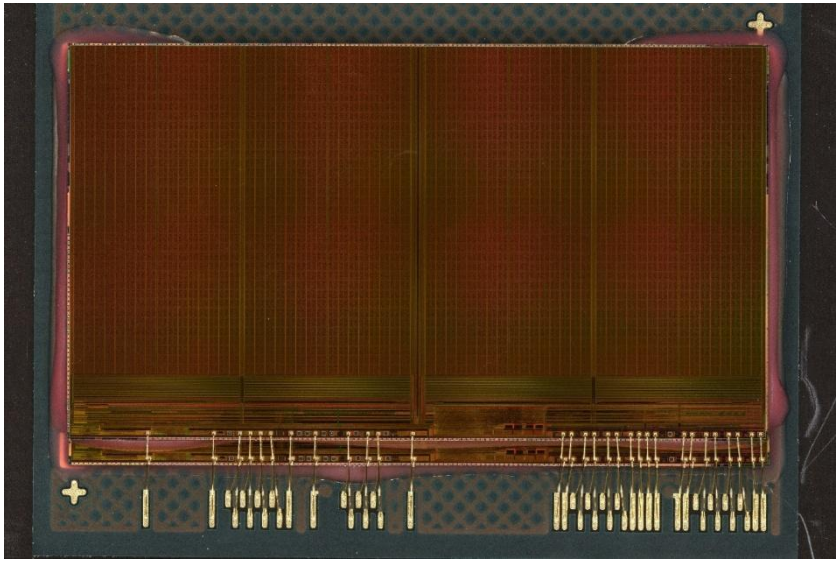


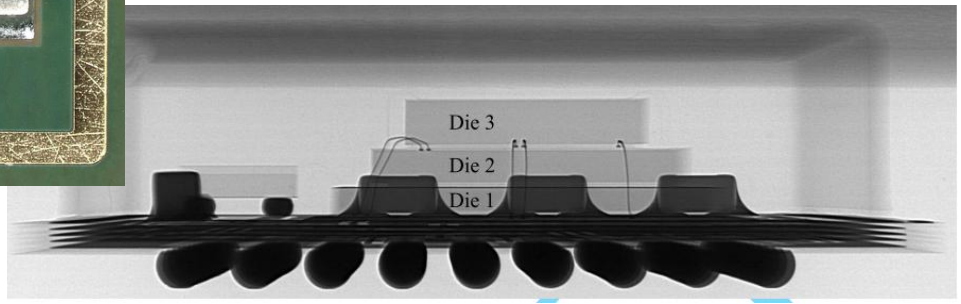


Flipchip dimension : 14550x6410um
Pitch TOP for flipchip 300um
Pitch BOTTOM for Ball Grid Array 800um
Minimum Line width 40um
Minimum Spacing 40um
Drilling for uvia TOP-BOTTOM 80um - Pad 180um
Filled Via on Pad with Cu

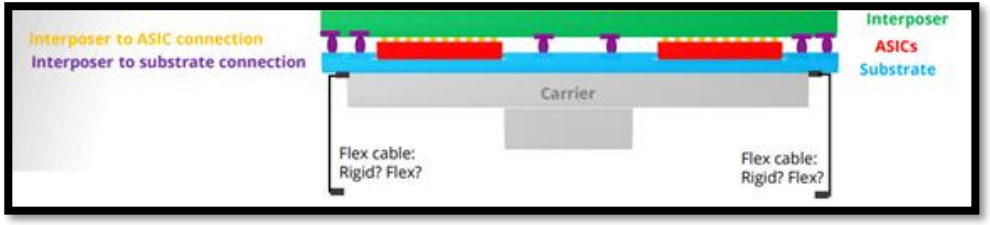
SIP USING STEPPED OR STAGGERED DIE STACKING





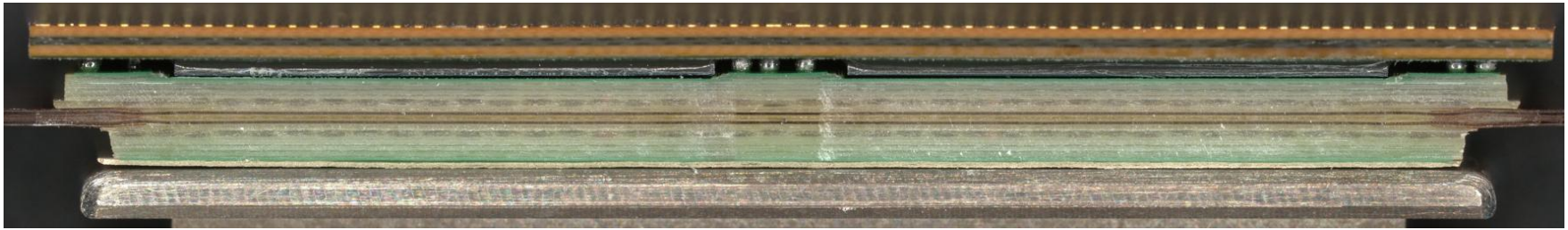


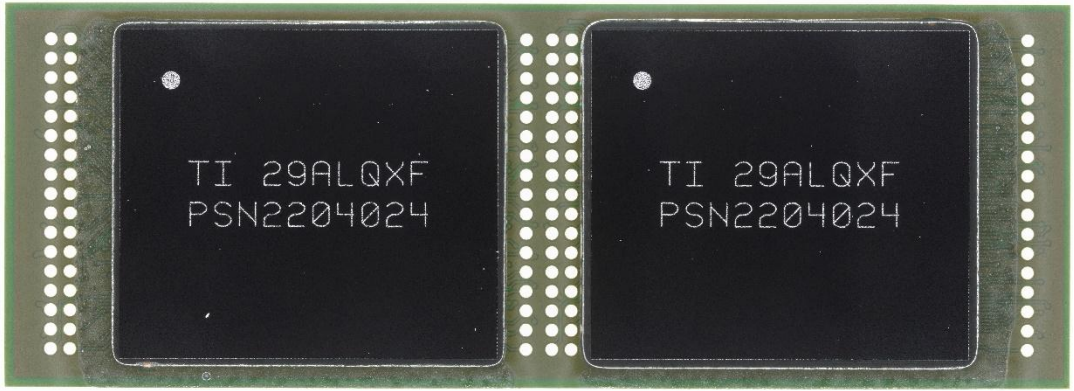
SIP USING EMBEDDED COMPONENT



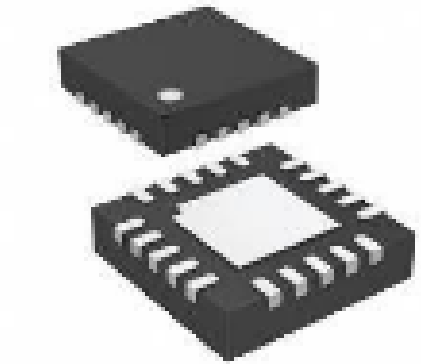
ASIC is :

- 8x7mm large
- Pitch is160mm
- I/O counts are 2260
- Bump Height is 63µm





LEADFRAMES PACKAGES



LQFP

- **Full In House - Assembly Line**

NEW IN

QFN

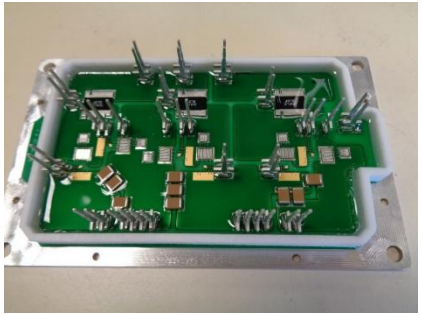
- All standard outlines available
- Standard Gluing & Sintering

POWER MODULES & RF PACKAGING

SERMA GROUP

AVAILABLE TECHNOLOGICAL BRICKS

SECURE YOUR FUTURE



SUBSTRATES

- Ceramic substrates (HTCC)
- Insulated Material Substrates
- AlN/AlN-DBC
- Si3N4
- AMB
- FR4 & Thick Copper PCB

DIE ATTACH

- Pressureless Silver sintering
- High Temp Soldering using convection or conduction

NEW IN

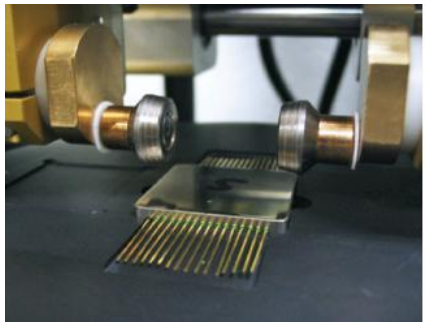
- Leadfree solder Paste (SnAg, SAC305) **USING VACUUM VAPOR PHASE**

INTERCONNECTIONS

- Heavy wire bonding (Al 125 to 400µm µm)

NEW IN

- **Clip Bonding ON DIE & DIE STACKING USING TOP METALLIZATION MODIFICATION (in house process)**

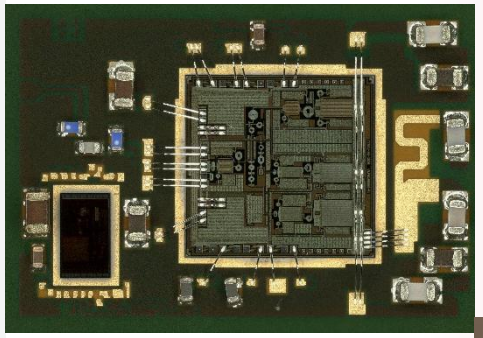


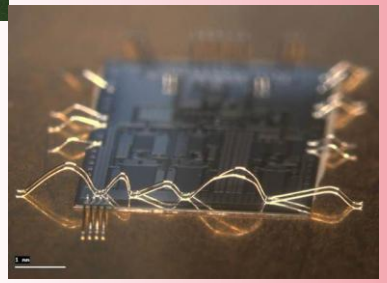
SEALING & SCREENING

- Seam welding
- Epoxy Glob top
- Silicon Gel casting

- Bond Pull / Die Shear
- X-Rays
- Seal test
- Laser marking
- Environmental tests (HTSB, TC,

SECURE YOUR FUTURE





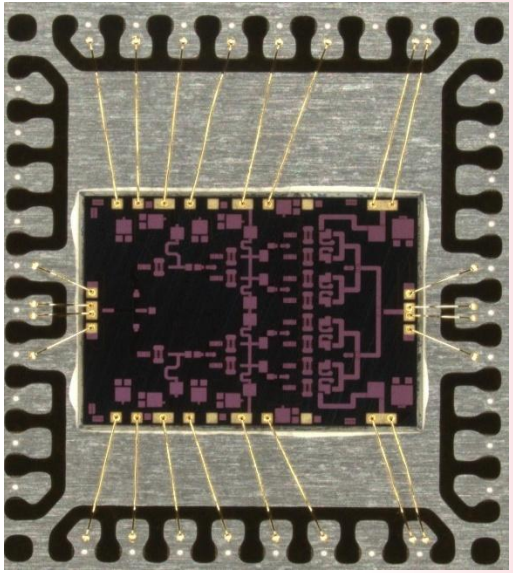
RF/MICROWAVE

SUBSTRATES DEVELOPMENT

- Organic substrates (Rogers)
- Thin Film Ceramic substrates
- Plastic QFN
- System in Package

ASSEMBLY TECHNOLOGIES

- Die & substrates attach:
  - Adhesive processing
  - Vacuum soldering
  - **Vapor phase vacuum soldering**
  - Silver sintering
- Wire Bonding:
  - Wedge Bonding: from 18µm to 50µm
  - Gold Bonding: from 18µm to 75µm
  - Length and form factor control
- SMT soldering
  - Chip size assembly down to 0201
  - SOP's, QFP's, BGA, **CSP's assembly down to 0,4 pitch**



GaN sur SiC in QFN

SOME ACHIEVEMENTS

TECHNOLOGIES INVOLVED

- Die & substrates attach:
  - Via filling
  - Adhesive processing
  - AuSn Vacuum soldering
  - Thin Film Manufacturing & Integration
- Wire Bonding:
  - Wedge Bonding: from 18µm to 50µm
  - Gold Bonding: from 18µm to 75µm
- Seam Welding
  - 30ppm @T0

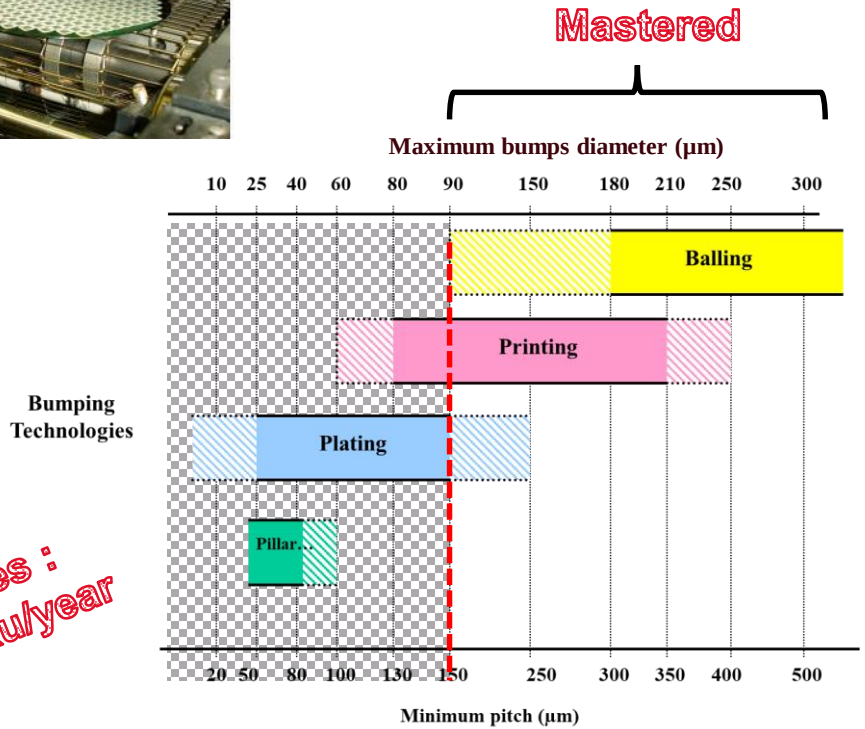
FLIP-CHIP CAPABILITIES

FOCUS ON WAFER BALLING & ASSEMBLY :

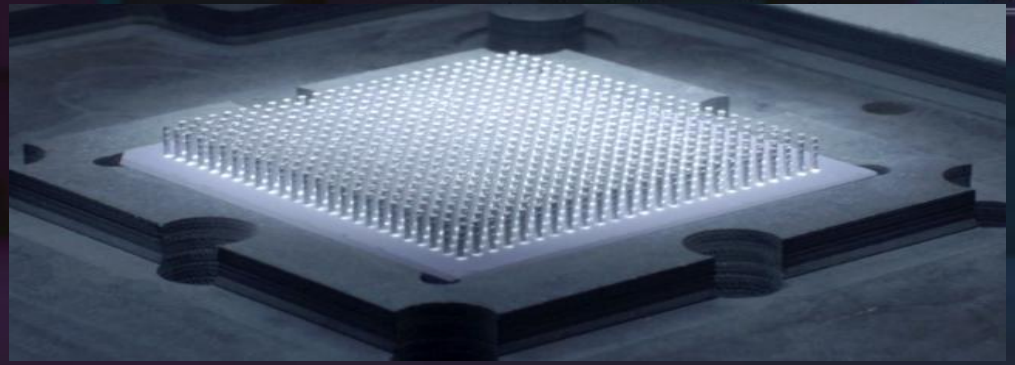
In-house Flip-chip manufacturing from wafer :

- **UBM (Under development in-house))**
- **Balling** process **(for bumps>300µm)** :
  - Screen print flux on wafer
  - Metal Mask
  - Balls : Sn63Pb37 or Sn95,5Ag4Cu0,5
  - Wafer reflow (convection)
  - Cleaning
  - Sawing
- **Printing** Bumping Process **(for bumps<300µm)** :
  - Solder paste screen printing on wafer
  - Balls : Sn63Pb37 or Sn95,5Ag4Cu0,5
  - Wafer reflow (convection)
  - Cleaning
- **QA control** :
  - XRAY inspection
  - Ball shear (JEDEC JESD22 TM B117B)
  - Dimension control with CNC video measuring system (NEXIV VMZ-R) :
    - Ball diameter (down to 80µm with a pitch of 120µm)
    - Coplanarity (min value is 60µm for 280µm balls)
- **Report on substrates** :
  - Solder paste or Flux screen printing on substrate
  - **Report on substrates using SET ACCURA PLUS**
  - **Reflow (Vapor phase or convection)**
  - Cleaning and contamination checking
  - Visual Inspection
  - x-rays using laminography
  - **Highest ball counts mounted for a flip-chip is 2260!**

Capabilities :
Up to 100ku/year



COLUMN ATTACH PROCESS



KEY POINTS OF OUR TECHNOLOGY

NEW IN : LEADFREE COLUMNS IN 2025

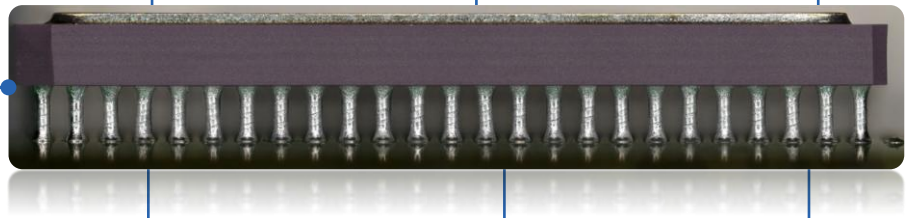
SECURE YOUR FUTURE

Short Lead-Time :
- ✓ 4 weeks for 50 CCGA625

Degolding & Tinning

Column soldering :
- ✓ Max thermal stress : 210°C
- ✓ Only one Reflow

R&T CNES 2022



Automatic Matrix filling

Qualified Rework

In-House Columns Manufacturing :
- ✓ Core wire is Sn15Pb85 or Sn80Pb20
- ✓ Reinforcing Material is Copper
- ✓ Tinning material is Sn63Pb37
- ✓ Diameter are : 0,38mm or 0,51mm (six-sigma like)!

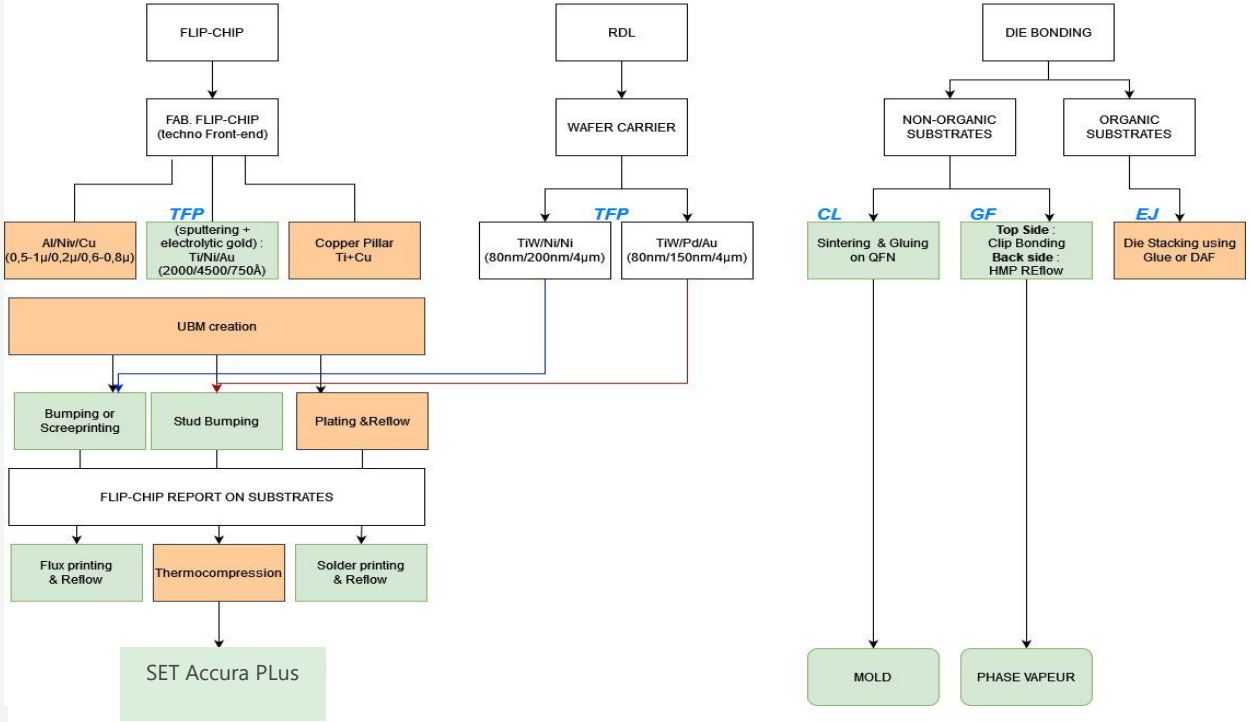
Quality control:
- ✓ 100% coplanarity control : Mean value is 80µm
- ✓ Columns 100% measured by height, diameter and pitch
- ✓ Visual Inspection per MIL-STD-883 : no diameter reduction higher than 20%
- ✓ Solderability tests per MIL STD 883 method 2003
- ✓ Column pull test per MIL STD 883 method 2038

* : depends on work load

ROADMAP & NEW DEVELOPMENTS

2023-2025 TECHNOLOGICAL ROADMAP

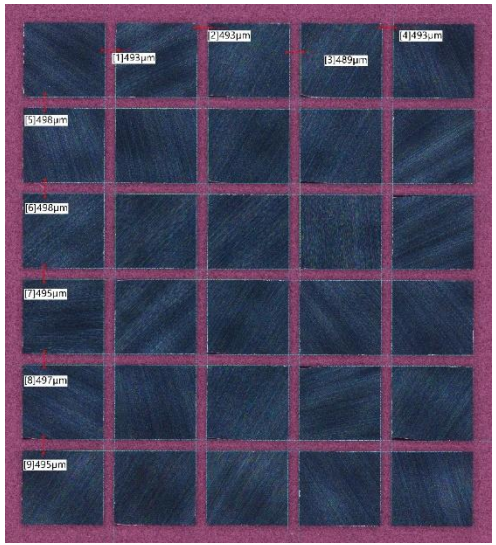
FOCUS ON DIE LEVEL PROCESS



	SOUS-TECHNOLOGIES		TRL
FLIP-CHIP PROCESS DEVELOPMENT	UBM sur wafer ou quart de wafer	Wafer bumping	6
		Stud Bumping	6
	UBM sur puce unitaire	Die bumping	6
		Stud Bumping	7
	Report des flip-chip sur substrats	Classic Reflow	8
		Thermo-compression	7
FAN OUT-FAN IN	RDL	Fan-In	5
		Fan-out	
DIE ATTACH	Die Attach Film for DIE STACKING		3
	Non-organic Susbtrates	Clip Bonding (die remetallization)	8
LEAD FRAMES	QFN		8
	LQFP		8

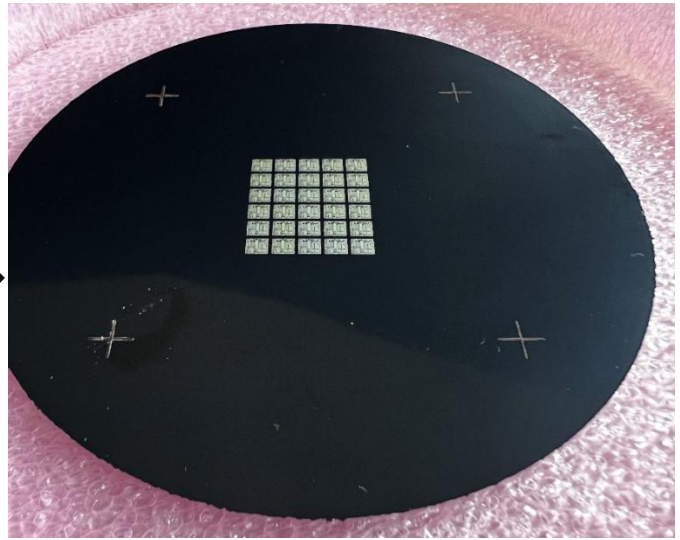
WAFER RECONSTITUTION FOR RDL OR UBM

SECURE YOUR FUTURE



Back side before molding

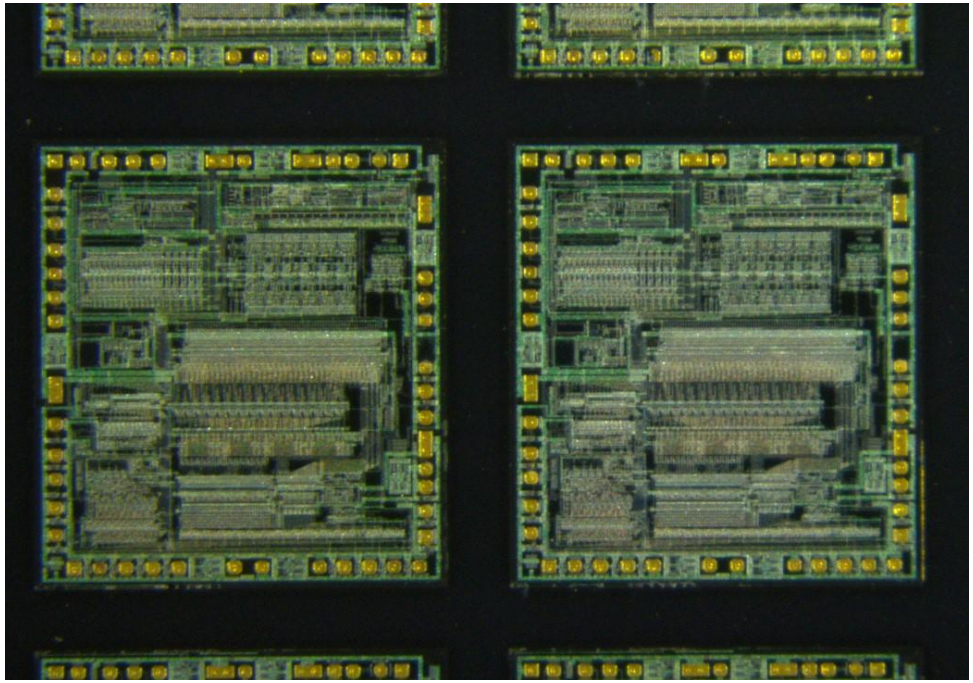
Top side after molding (300µm)

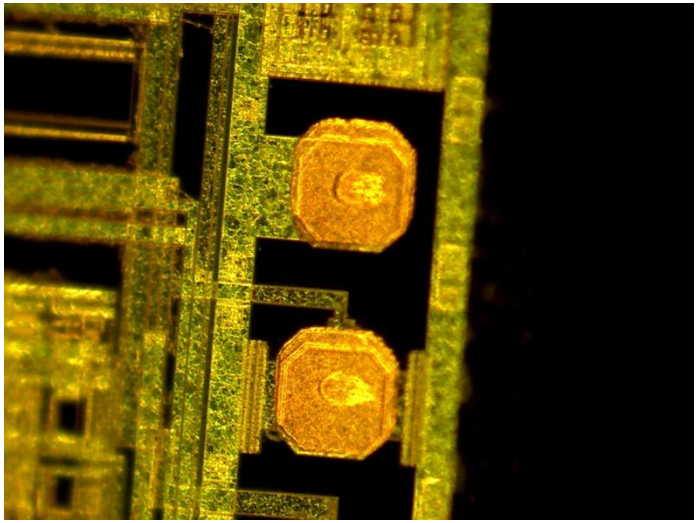


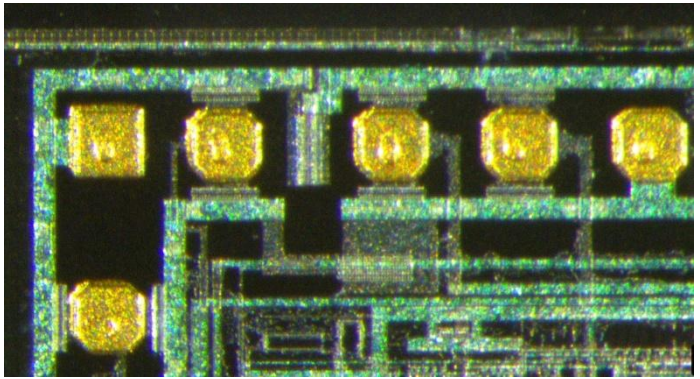
Wafer reconstruction

Our Ambition : Bumping & RDL services for singles dies and for ow (10) to Medium volumes (5k)

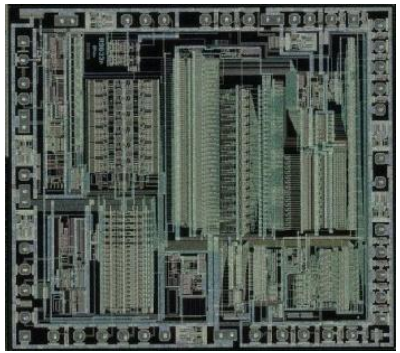
ZOOM ON RDL OR UBM



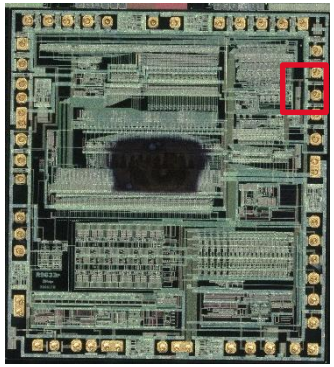




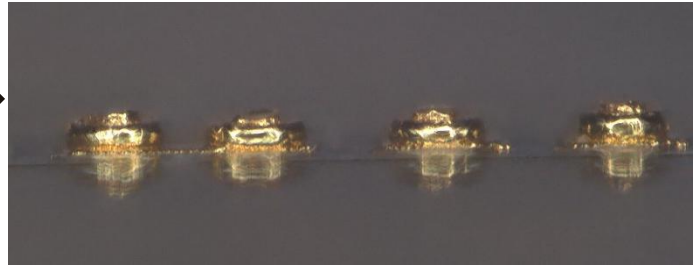
UNDER BUMP METALLIZATION



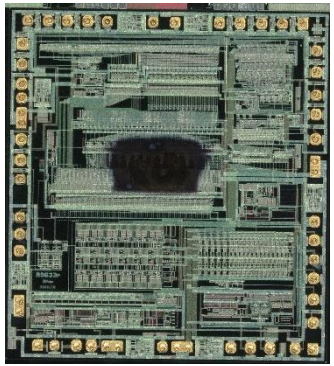
AlSi pads
80 x 80 µm



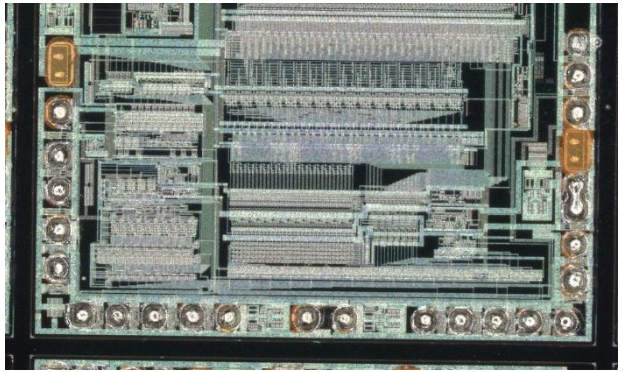
Thick Gold metallization



Stud bumps using 25µm

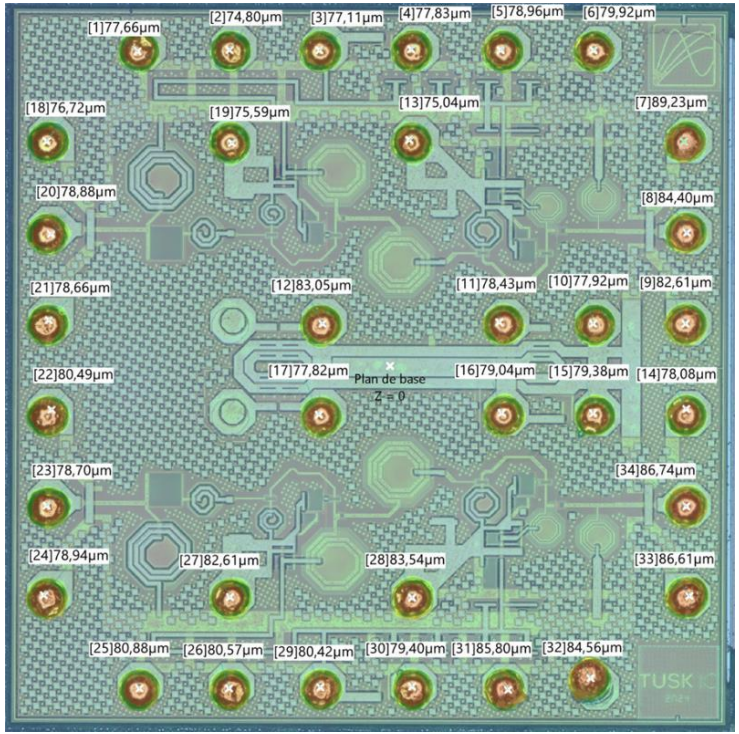


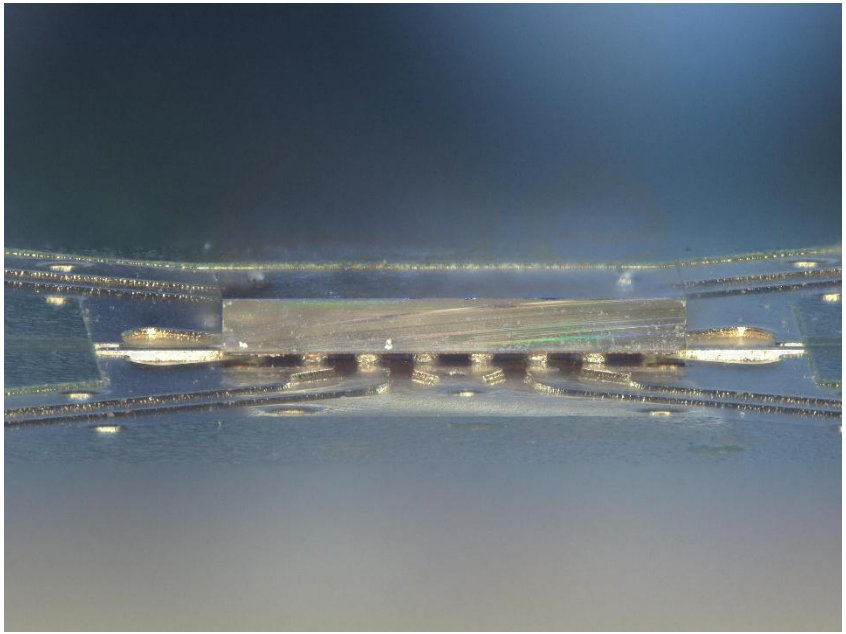
Thin Gold metallization



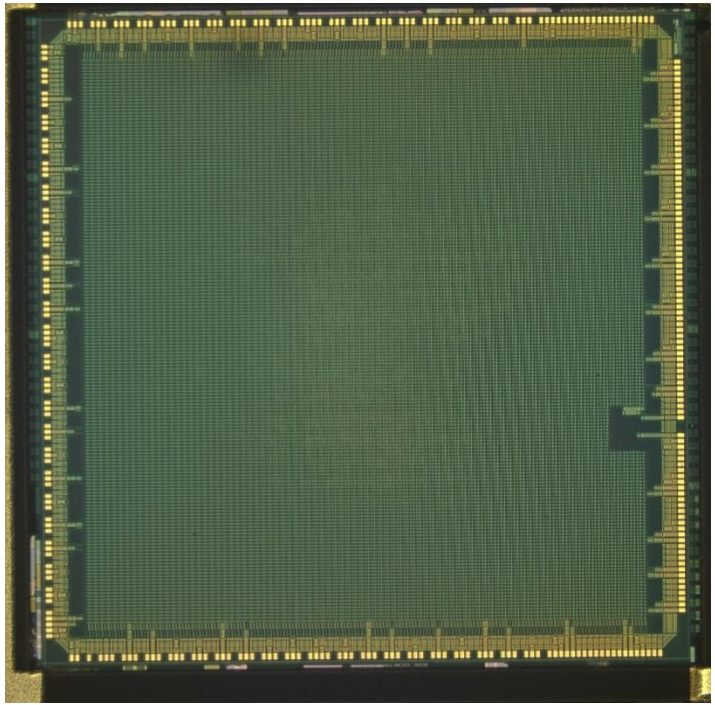
Balling

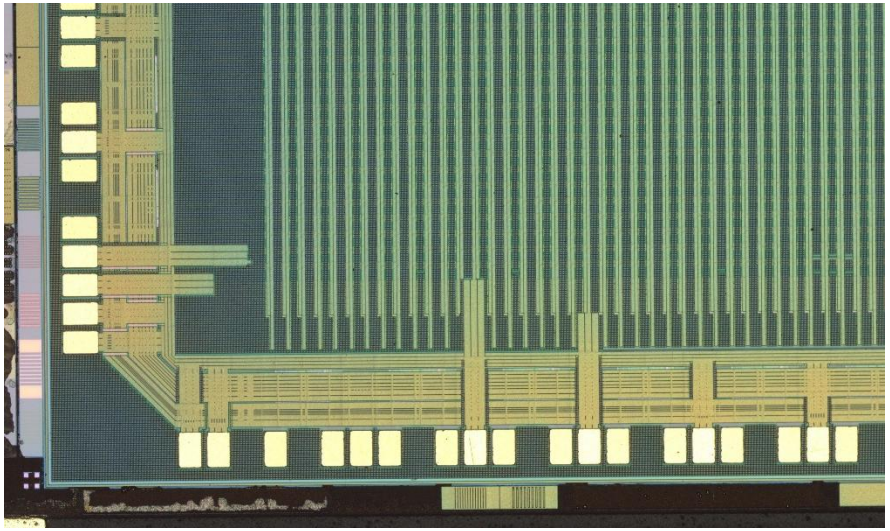
UNDER BUMP METALLIZATION (UBM CREATION ON 2'' SUBSTRATE))



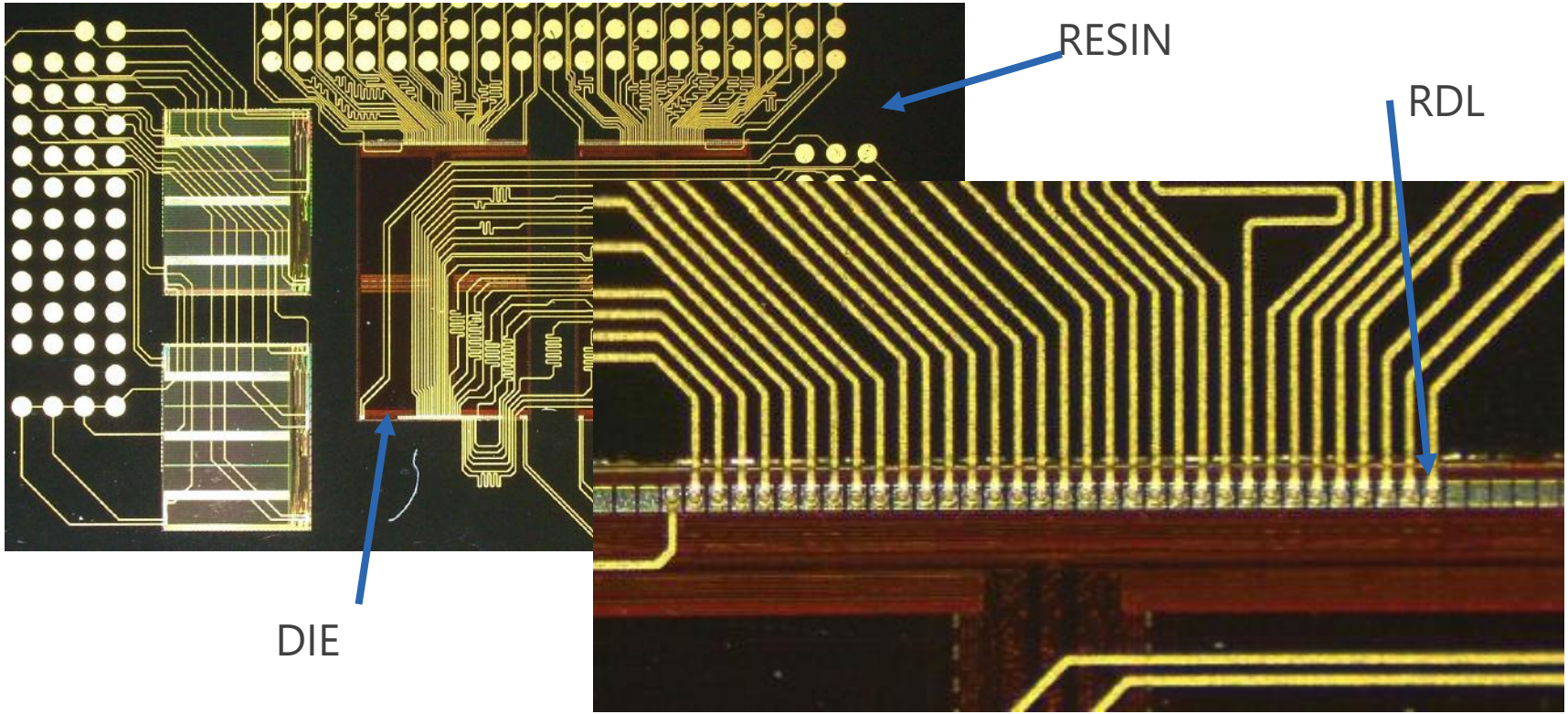


UNDER BUMP METALLIZATION (ON 10X10MM DIE)

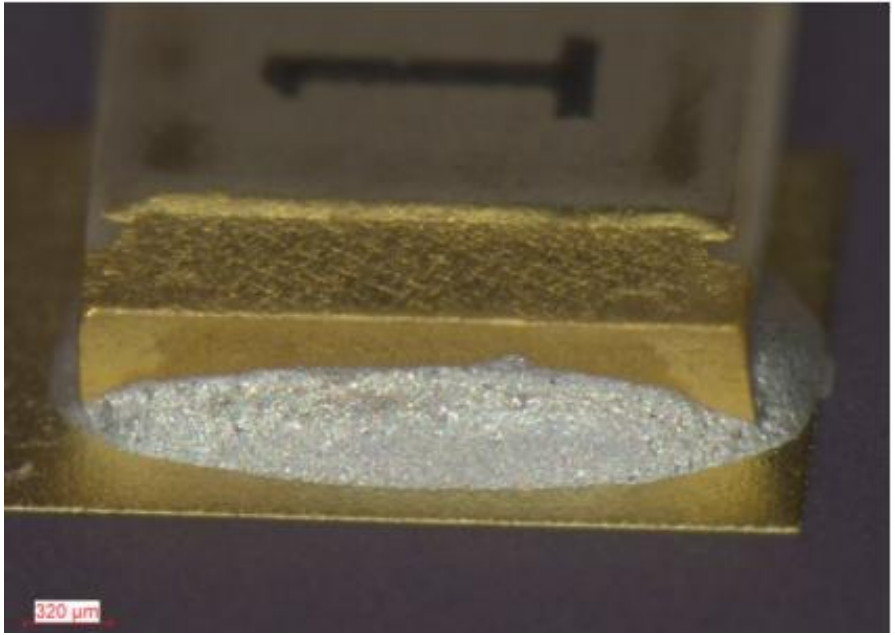


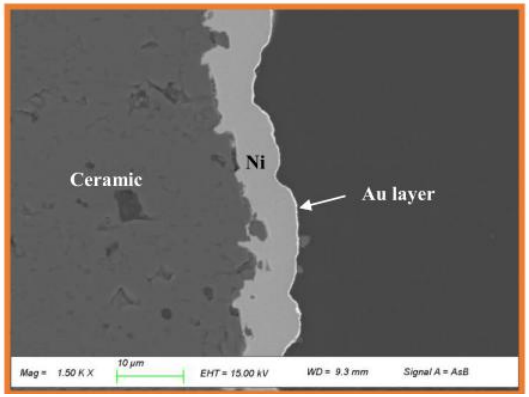


REDISTRIBUTION LAYER (FAN-IN & FAN-OUT RDL



SMD REMETALLIZATION FOR BRAZING & GLUING PROCESS

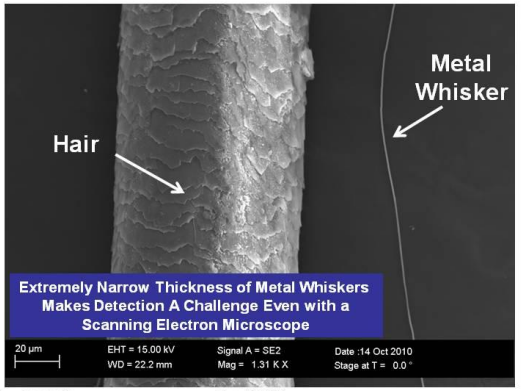




After stripping of Sn, Gold layer is deposited on pads over Ni layer to avoid **Whiskers and Reliability Issues**

Human Hair vs. Metal Whisker

Metal Whiskers are commonly 1/10 to < 1/100 times thinner than a human hair!!!



OPTOELECTRONICS & PHOTONICS PACKAGING

SERMA GROUP

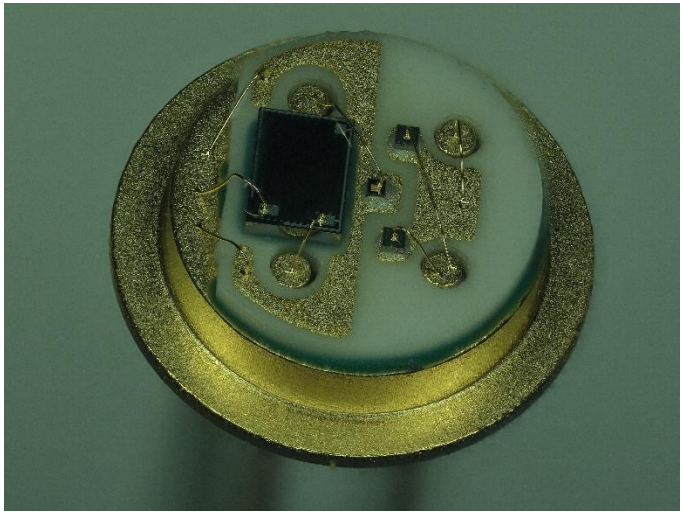
OPTOELECTRONICS

Assembly line (class 100/IOS5) dedicated to optical devices :

- Automated Die placement accuracy : +/- **0,3µm (ACCURA+)**
- Glass Lid Brazing
- Parallelism control <50µm
- Programmable Epoxy dispensing pattern
- Thermal or UV snap cure
- Hermetic Seam Sealing in inert N2 environment
- <5000ppm moisture content

Key Areas of expertise:

- Solutions for a wide range of devices and wavelengths including VCSEL's & Photodiodes
- Wide range of packages including TO-CANS.

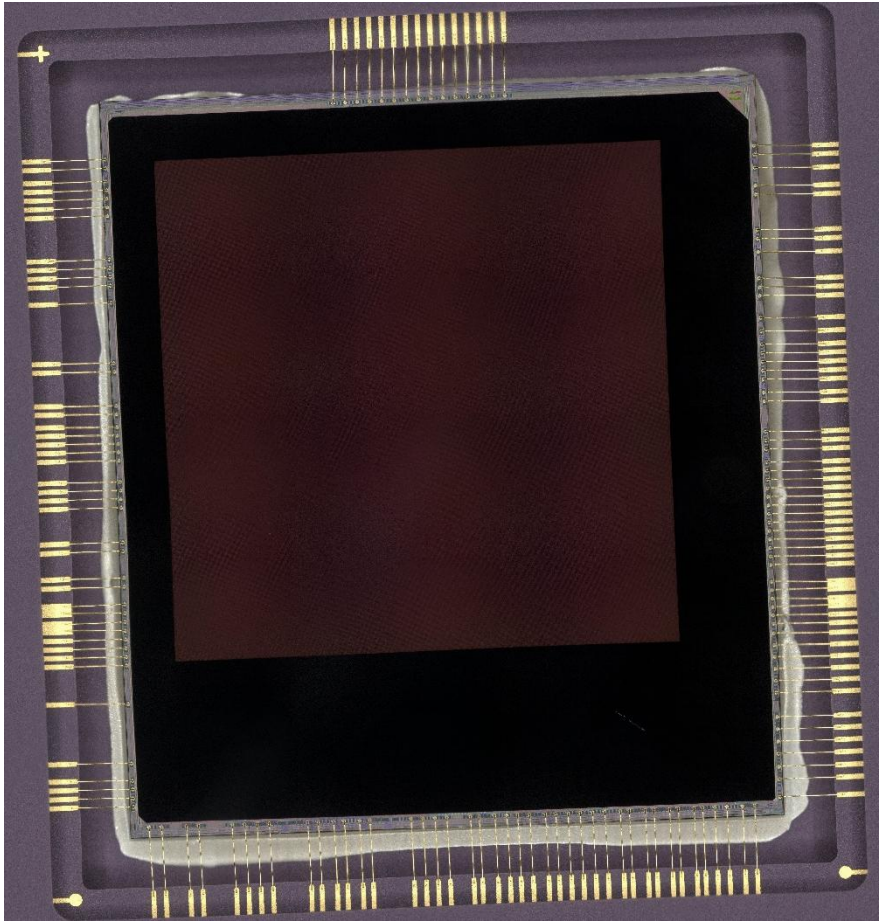


OPTOELECTRONICS

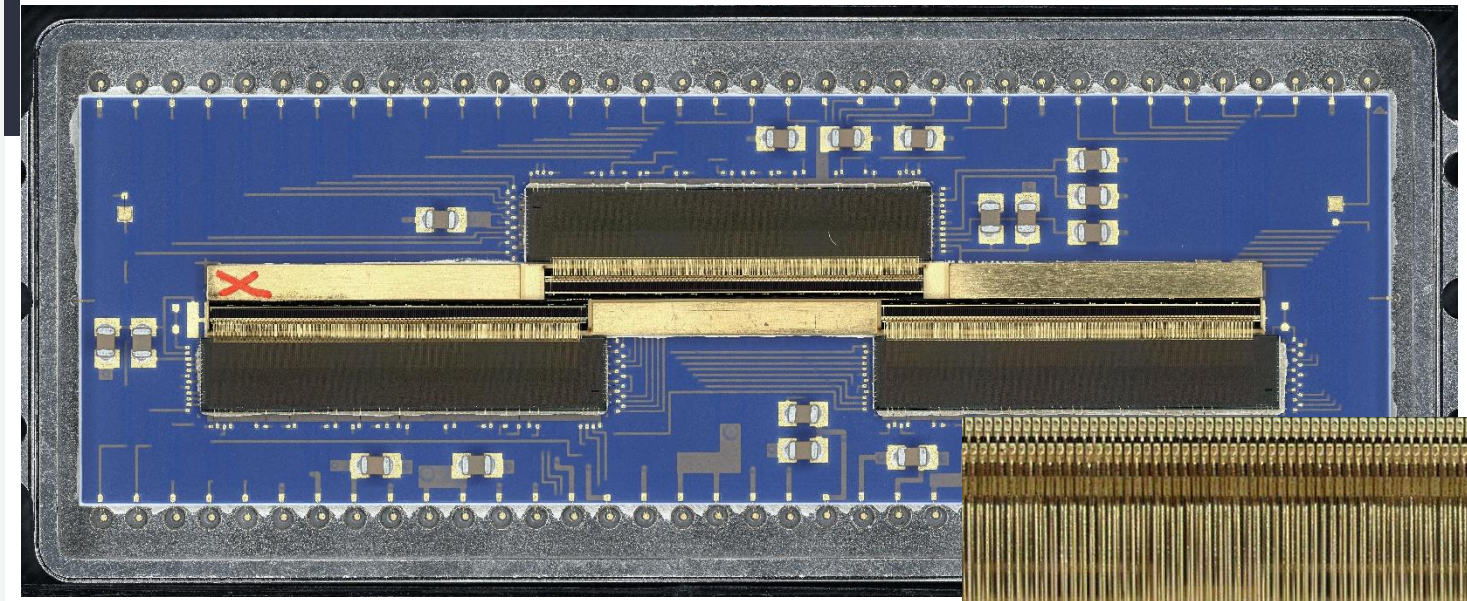
Process Highlights on :

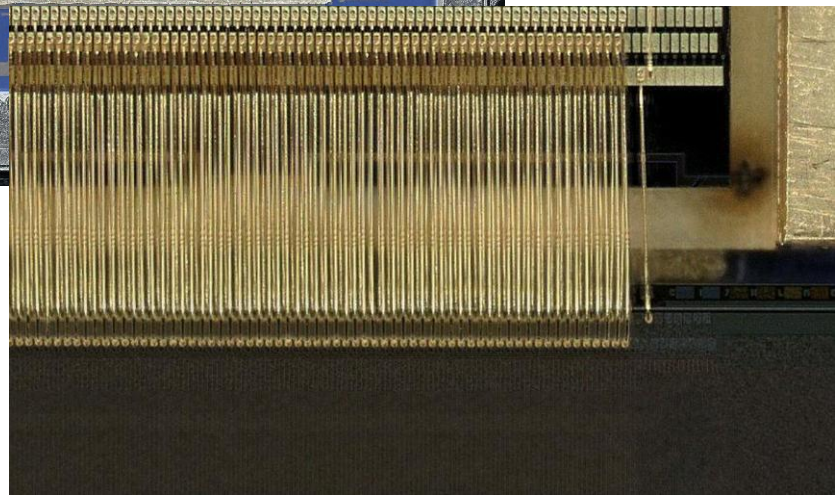
- **Space Heritage for C-MOS Imaging Sensors**
- Full ESCC9020 screening and qualification
- Molecular Cleanliness : lower than 0,5 mg/m²
- Particulate Cleanliness : lower than 100 ppm

- Automated Die placement accuracy : +/- **0,3µm (ACCURA+)**
- Rotation control < 0,1°,
- Parallelism control <50µm
- Programmable Epoxy dispensing pattern (coverage>75%)
- Thermal or UV snap cure
- Glass attach with Hermetic Seam Sealing in inert N2 environment (<5000ppm moisture content)



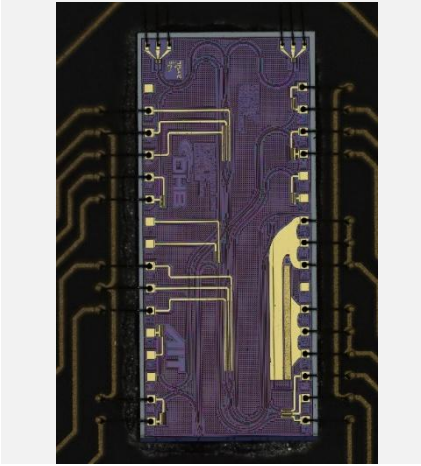
INFRARED SENSORS ASSEMBLY





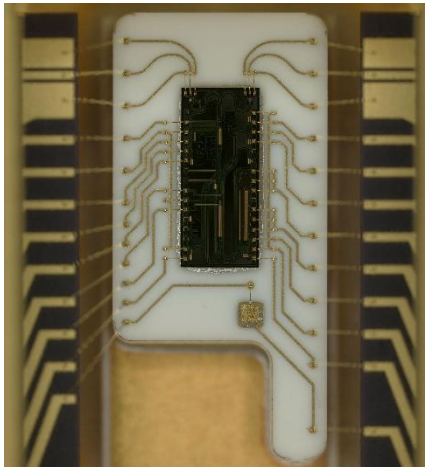
- Detector & ROIC Dies Assembly
- In-house Thick Film substrate Manufacturing
- Passive soldering
- 2700 wires bonding (17µm & 25µm)

PIC ASSEMBLY FOR SPACE PROGRAMME



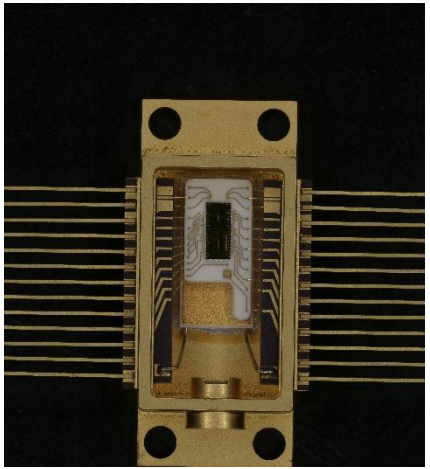
DIE INSPECTION

Visual Inspection Level A according to MILD-STD-883, ISO-5 environnment.



ASSEMBLY

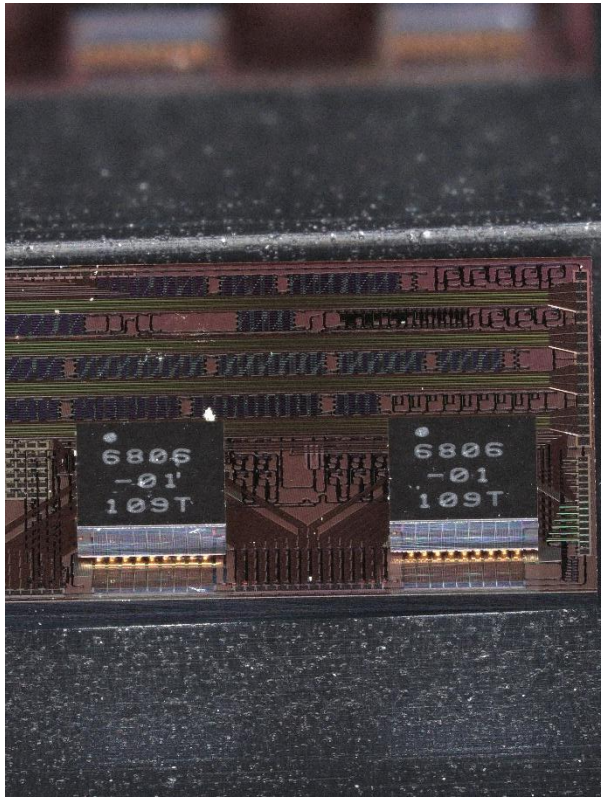
Die attach with conductive glue and wirebonding with Au 25 µm wire.

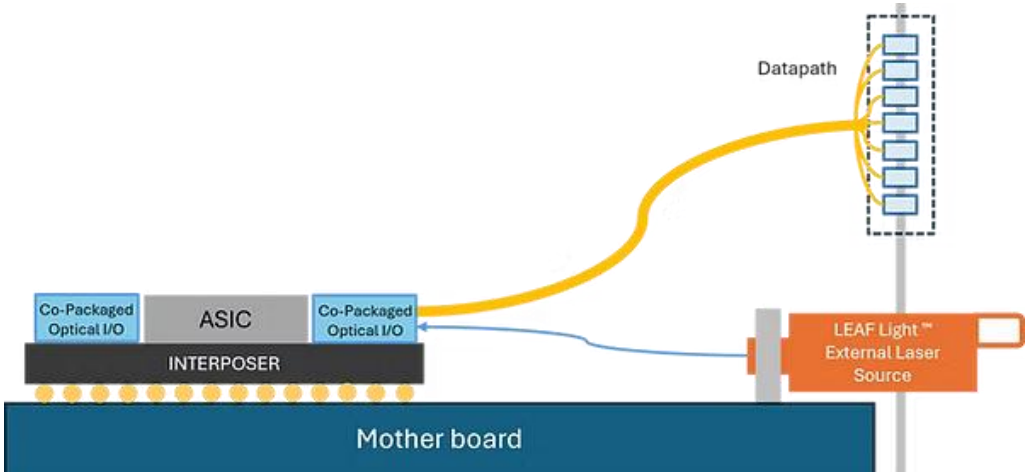


SCREENING

Hermectic sealing, fine & gross leak, constant acceleration, PIND test, electrical test, Burn'In.

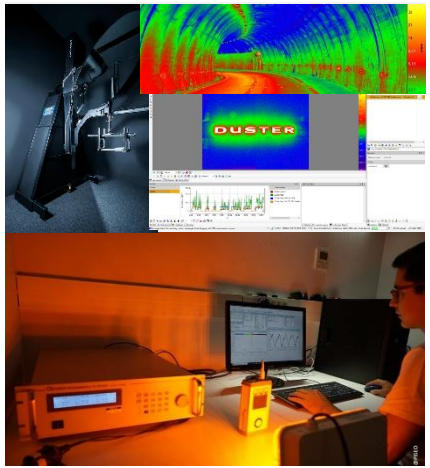
CO-PACKAGED SILICON PHOTONICS





RECENT INTEGRATION OF PISEO INTO SERMA GROUP !

PISEO
photonics.innovation.services

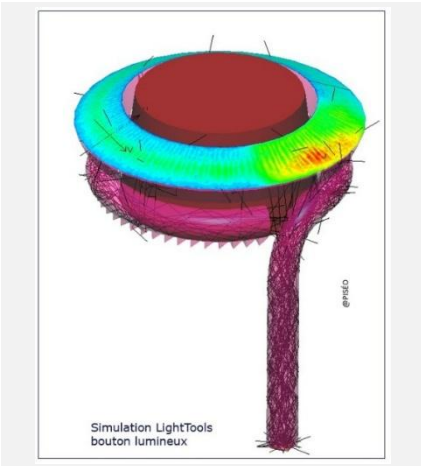


PHOTOMETRY LABORATORY

Luminance, photometry, flow, colorimetry, optical flicker, stroboscopic effect, radiometric in the UV measurements.

OPTICAL IMAGING LABORATORY

FTM, Geometric distortions, Signal-to-noise ratio, Depth of field and field of vision, Sharpness, Luminance, uniformity and contrast, Colorimetry gamut, Dark current, NUC



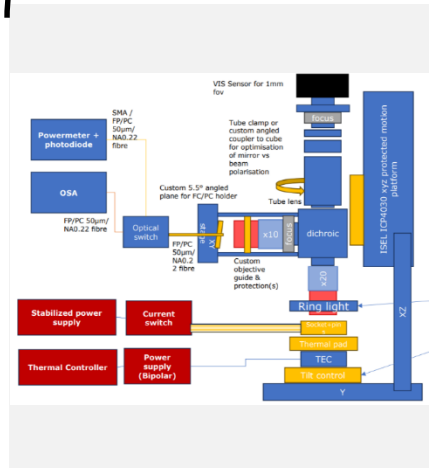
OPTICAL DESIGN AND SIMULATION TOOLS

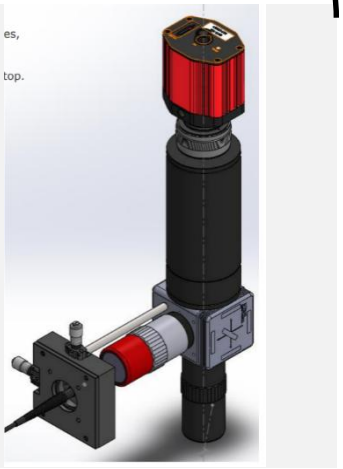
PISEO has state-of-the-art optical design and simulation tools. They represent an undeniable asset for optical design.

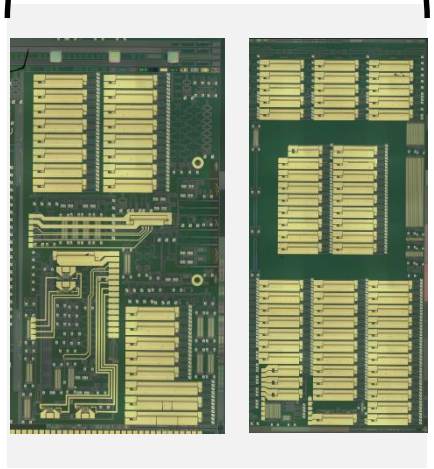
CHIP CARACTERIZATION

PISEO photonics.innovation.services

SERMA MICROELECTRONICS







ARCHITECTURAL STUDY

Instrumentation research work, feasibility with the customer. Architecture review report.

DEVELOPMENT / ASSEMBLY

3D development, instrument programming, HMI development. Test bench set-up.

CHIP ASSEMBLY & CHARACTERISATION

Die attach on thick film substrat, wirebonding of grading couplers with Au 25 µm wire. Dam&Fill to protect the wires.

R&D PROJECT 2024-2025

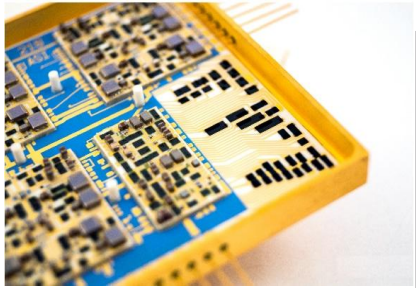
SERMA GROUP

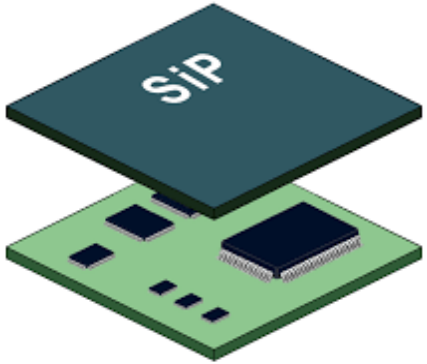
SYNTHESE PROJETS R&T
SERMA MICROELECTRONICS

- **Hermetic System-in-Package**
- **Hermetic Power Modules using Clip Bonding & Parylene**
- **Chip Scale Package Technologies**
- **LeadFrame Type Package : QFN and LQFP**

HPM PROJECT

HERMETIC HYBRID MODULE :
High realibility





System-in-Package :

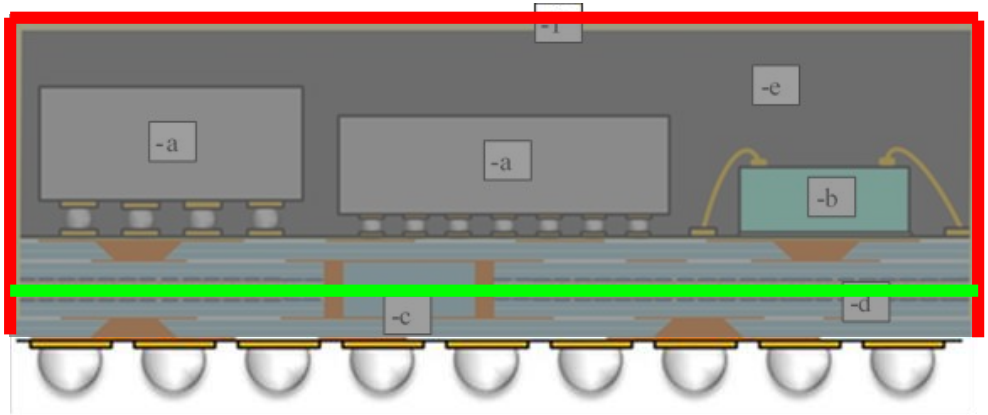
High density
- Organic substrate
- SMD product

Cheaper, but non-hermetic manufacturing processes

HPM PROJECT → **Hermetic Solution for SiP (organic substrate and plastic component)**

HERMETIC PLASTIC BGA PACKAGES

METALIZATION



SiOx material integreted

BRIDGE RECTIFIER MCM HI-REL

SECURE YOUR FUTURE

Die clip bonding

Die plating change from Al to Ag

Jumper design for High power use

Original Al plating

Specific design

Hi-Rel HTCC custom design with multi-chip

High power

High integration level

Qualification

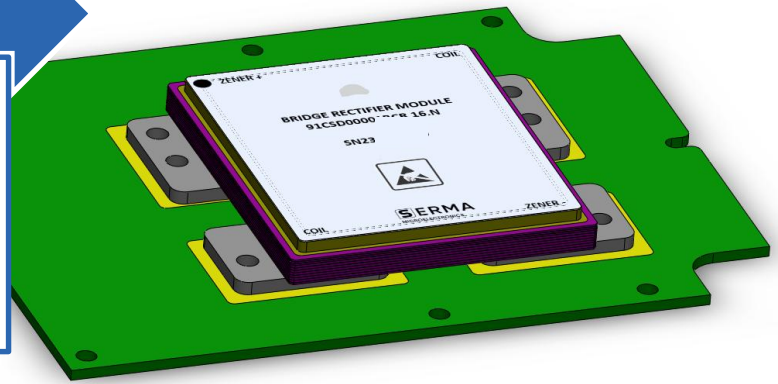
Fast prototyping demonstrator

Thermal simulation

Power testing

Industrialization

Customer support for final use



MAIN INVESTMENTS 2023-2024

Vacuum vapor phase (April 2023)

- SMT soldering on SiP
- Voids reduction (<1%)
- Capacity increase vs BGA balling

X-Ray machine (Q4 2023)

- Equipment replacement
- Resolution improvement
- Voids rate detection
- Laminography (die attach control)

Die attach System (Q4 2024)

- Backup for current equipment
- Capacity increase

SECURE YOUR FUTURE

MAIN INVESTMENTS 2025 - 2026

Electromagnetic Weld Head
- Parallel Gap
- Thermocompression

300mm Automatic Dicing Saw(Q4 2026)
- Up to 12 inches wafer processing
- Capacity increase

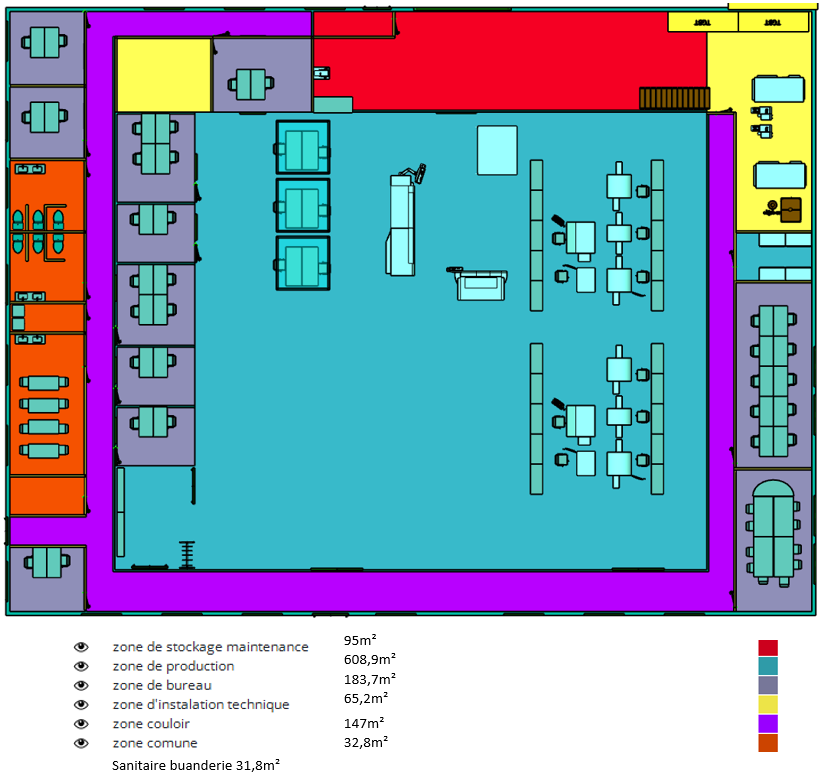
Processes to be addressed in 2025 :
- Flip-chip pick & place
- Glass Frit
- UV glue Polymerization (optical assy)
- Die-on-Die Placement with accuracy: +/-3 µm
- Die on wafer
- Thermocompression

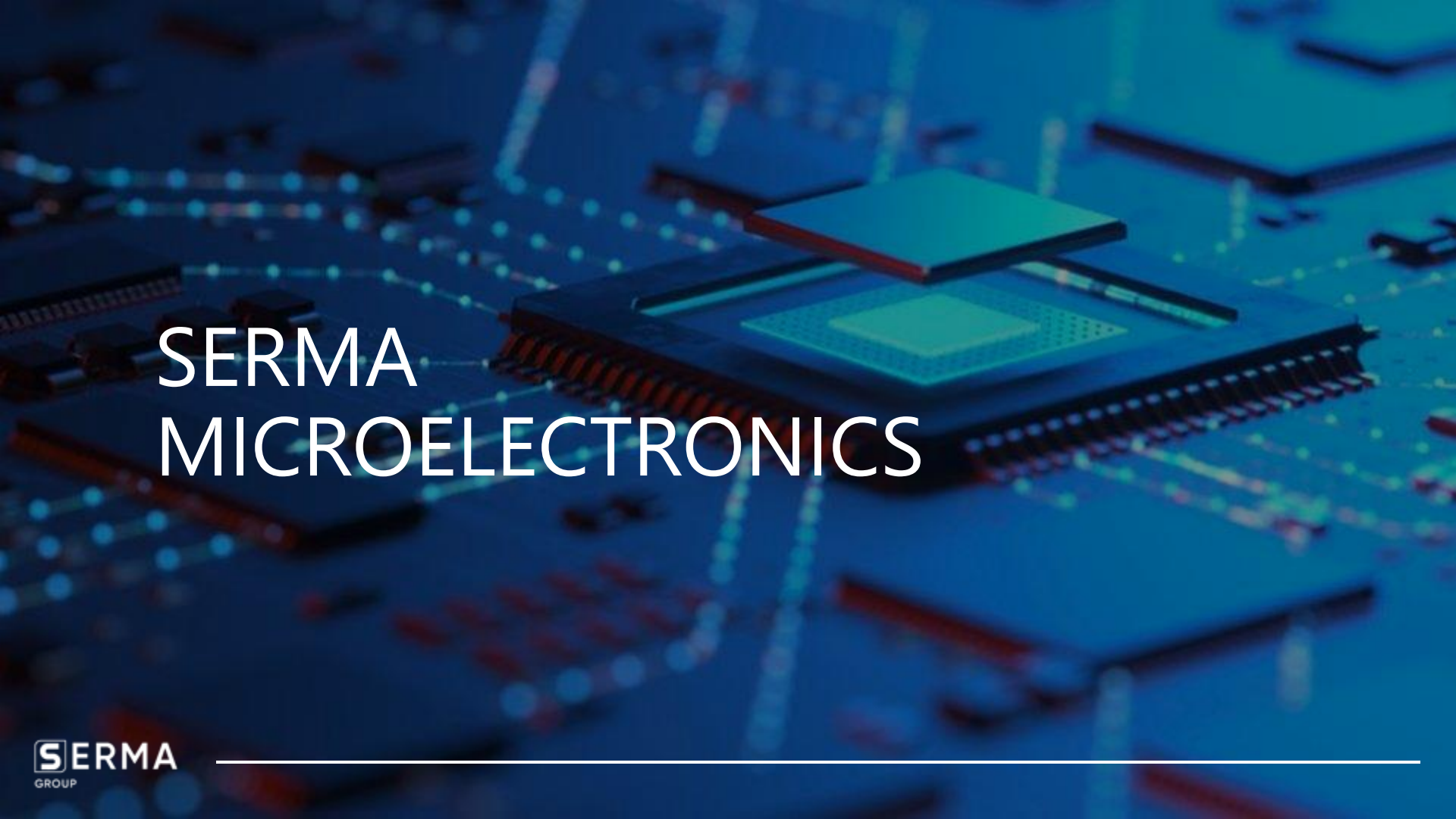
NEW BUILDING : 2025-2030

SECURE YOUR FUTURE

BUILDING PERIGNY 2

- New production area
- 800 M2
- AVAILABLE September 2026
- Total surface area after construction Perigny1 + perigny2 = 3200 M2





SERMA MICROELECTRONICS

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